VIGNAN'S
Foundation for Science, Technology & Research
(Deemed to be UNIVERSITY)
-Estd. u/s 3 of UGC Act 1956

R22 Academic Regulations

In Compliance with NEP 2020

Prof. P. NAGABHUSHAN
B.E., M.Tech., Ph.D., FIE, FIETE, FIAPS.
Vice Chancellor, VFSTR
Life time Professor, IIIT – Allahabad, Prayagraj
(Formerly: Director, IIIT-Allahabad 2017-22)

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PREFACE

'You are born to Blossom' – What an inspiring title the book authored by APJ Abdul Kalam and Arun K Tiwari carries. The journey to blossom has got to be heralded by education. The purpose of education is to ensure that the 'Life Blossoms'. Earning a degree and getting a placement should be the just happening things, and should not become the only celebrated goals for education. In the book cited above, Honourable Kalam, Former President of India, underscores that "The scheme of civil society depends on Educating young people to become enlightened citizens and adults who are responsible, thoughtful and enterprising"

VIGNAN aims to seed these concepts in every learner who transits through this temple of learning. The doctrine of VIGNAN entitled R-22 contains the principles of policies laid down by the University, to realize the spirit of "Blossoming the lives" providing a foundation-strong professional education on the ethos of 'Creative learning for Critical thinking and Critically analysing for Creative decision making'. Certainly, our University is one of the earliest Universities, in fact the University is a trend setting one in completely internalising the concepts of the policies brought out in National Education Policy (New Educational Policy) NEP-2020, and inculcating the spirit in R-22. The R-22 document articulates the Academic Regulations of the University, which is being presented now and shall be inforce with immediate effect from the academic year 2022-23, not only for those who have joined in 2022, also the aspirants of 2021-22 are enabled into the navigation.

R-22 presents a novel design for the academic pursuit, making an exploratory cross disciplinary traversal for a learner who should find learning both holistic and experiential. The learner is ensured to enjoy the continuity in learning and the learner is supported to align and realign, enroute utilising the benefits of constructive feedbacks that s/he receives because of continuous assessment. S/he will be empowered to enjoy the opportunities to explore, experiment and experience.

R-22 eliminates the melancholy of examinations. The expected severity of breakdown due to the anxiety of examination system is replaced by an affectionate assessment system, increasing the effectiveness in accomplishing the outcomes.

In brief, NEP-2020 compliant revised academic regulation of the University – the R-22, is VIGNAN's commitment to alleviate the acuteness in the present educational practices. It intends to provide a strategic solution to the critical observation made by Bharat ratna awardee, Professor. CNR Rao – "India has exam system, not education system. When will young people stop taking exams and do something worthwhile?" (Thought for the Day, Times of India 13.08.2022)

Here is R-22, which assures that the learners at VIGNAN are bound to do something worthwhile – very much worthwhile.

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R22 M.Tech.
2 YEAR
PG PROGRAMME

REGULATIONS - TABLE OF CONTENTS

* Programme will be offered based on satisfactory strength of students willing to register, after receiving the formal AICTE approval.

R22 M.Tech. 2 YEAR PG PROGRAMME

Academic Regulations, Curriculum and Course Contents

R22 M.Tech. 2 YEAR PG PROGRAMME

EXECUTIVE ABSTRACT

R22 - Academic regulations, Curriculum and course contents, is an articulation of the VFSTR deemed to be University's commitment towards NEP-2020, with a view that it enables student(s) to maintain the spirit of continuous learning and continuous assessment to replace the normal tendency of preparing just before a test or an examination. The proposed framework accomplishes multi-disciplinary holistic education, continuous assessment along with multiple honorable exit options if a student falls short to complete the requirements to earn the degree within the stipulated period including the permissible spill over period.

R22 is oriented towards holistic education at the postgraduate level that includes integrated and rigorous exposure to professional domains, as well as sufficient flexibility in curricular structures that allow students to choose electives from the wide choice of courses. Such holistic and diverse education will assist the candidate in transforming into all-rounded persons. Similarly, in line with NEP-2020, more weight is given to continuous/ formative assessment, in the frame work of an Integrated learning model comprising Learning – Thinking – Understanding – Skilling – Applying – Creating. Emphasis on continuous formative assessment with a creative summative assessment will facilitate the candidate to "Move away from high stake examinations – towards more continuous and comprehensive evaluation".

The M.Tech. degree offered will be for two years' (4 semesters) duration with lateral exit options within this period, with suitable certifications that will enable the candidate to have a professional career and as well as serves as a reminder to return and update his / her qualification in the future. In line with NEP-2020, following one year of study and the completion of the required credits, an Engineering PG Diploma degree will be conferred. However, the intention of the learners is not to join for the award of the PG diploma with lateral exit, but to acquire a M.Tech. degree.

Salient features of the regulation

- Continuous learning
- Continuous assessment
- Add-on certification
- Honorable exit option
- Onward Continuation to Ph.D. Program
- Sabbatical Semester Drop option to pursue innovation, incubation, entrepreneurial and advanced exploratory activities and subsequent re-entry

1 INTRODUCTION

This document contains the academic regulations, scheme of assessments, curriculum, detailed syllabi, course contents with text / reference books recommended, course outcomes, skills acquired and the projects / assignments that are to be performed for each course for the conduct of 2-year M.Tech. degree programmes. The various M.Tech. degree programmes under different schools in VFSTR are as listed below. The character codes indicated in paranthesis are their branch disciplinary code.

I. School of Agriculture & Food Technology

- Food Processing Technology (FT)
- Farm Machinery (FM)

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II. **School of Biotechnology & Pharmaceutical Sciences**
- Biotechnology (BT)

III. **School of Computing & Informatics**
- Computer Science & Engineering (CSE)

IV. **School of Conventional Engineering**
- Structural Engineering(SE)
- Machine Design (MD)

V. **School of Electrical, Electronics & Communication Engineering**
- Embedded Systems (ES)
- VLSI (VLSI)
- Power Electronics and Drives (PED)

1.1 Definition

For the purpose of R22 regulation, definitions as follows shall apply:

- **"Degree"** shall refer to the M.Tech. Degree Program.
- **"Course"** shall refer to such Course(s) for which a student shall earn Credits after due assessment as per the laid provisions. Project is also treated as a Course.
- **"Academic activities"** shall refer to the activities like Lecture (Physical Lecture Session), Tutorial (Participatory discussion / Self-Study / Desk Work / Quiz / Seminar Presentation, *etc* activities that make the student absorb & assimilate, the delivered contents effectively) and Practical / Practice sessions (includes Hands on Experience / Lab experiments / Field Studies / Case Studies *etc* activities that enable the student to acquire the requisite skill).
- **"Continuous Assessment"** shall refer to the assessment of the student spread over the entire semester on the various constituent components of the prescribed course.
- **"Semester"** shall refer to a period covering the two assessment periods *viz* Formative and Summative Assessment period. A semester would generally be spread over twenty weeks.
- **"Course Drop"** shall refer to a student having to undertake a repeat of the Course(s) not being able to complete the Credit requirements of the Course(s), under the conditions stipulated in the regulation.
- **"Supplementary Examinations"** shall refer to the examination(s) conducted to allow the student to appear in the un-cleared Semester - End summative assessment component.
- **"Blank Semester"** shall refer to a Semester in which a student either does not register for any course at the beginning of the Semester OR chooses to DROP all courses OR is so compelled to DROP all the courses, as the case may be.
- **"Semester Drop"** shall refer to availing a blank semester. However, if drop is availed to pursue a creative extension activity, then it is defined as **semester sabbatical**.
- **"Spill Over Semester"** shall refer to the additional semester(s) beyond the completion of prescribed normal semesters.
- **"AAA Section"** shall refer to the Academics, Assessment and Awards Section of the Institute.
- **"Attendance"** refers to the Physical personal presence in an academic activity session.
- **"Summer Semester"** refers to a Semester that is scheduled to be held during the intervening period of Even and Odd Semester (*i.e*. Summer Vacation period).
- **"Themes"** refer to the courses offered in a particular stream other than offered by the regular departments, for example NCC, Entrepreneurship, Fitness and Living, *etc*.
- **"School"** refers to a division of institute dealing with two or more specific areas of discipline / study comprising of the departments related with exclusive emphasis on trans-disciplinary research.
- **"Department"** refers to a division of institute dealing with a specific area of discipline / study.

- **"HoD"** refers to the Head of the respective Department, where the student is enrolled for his / her Branch of Study.
- **"Center"** refers to a structured unit within the school / department established with the purpose to carry out advanced research.
- **"Grade Point"** refers to the quantification of the performance of a candidate in a particular course as defined herein.
- **"SGPA"** refers to the Semester Grade Point Average and is calculated as detailed in the regulations subsequently.
- **"CGPA"** refers to the Cumulative Grade Point Average and is calculated as detailed in the regulations subsequently.
- **"Division"** refers to the Division awarded to the student as per the mechanism detailed in the regulations subsequently.
- **"Internship"** refers to onsite Practical Training offered by reputed companies / Institutions, in India or abroad. To be undertaken with (or seeking) prior approval of the respective HoD.
- **"Project"** refers to a course executed by a candidate on a specific research problem at VFSTR / any organization of repute. To be undertaken with (or seeking) prior approval of the respective HoD.
- **"Credit equivalence and credit transfer committee"** refers to the committee designated to look into for credit equivalence and credit transfer.
- **"Honorable Exit Option"** refers to the Exit Options available to students, when they are unable to complete the prescribed two-year M.Tech. Degree program in four successive years.

1.2 Academic Administration

The academic programmes of VFSTR are governed by the rules and regulations approved by the Academic Council from time to time. The various academic activities are conducted following a fixed time schedule duly approved by the Academic Council in line with the AICTE / UGC regulations. The academic activities of VFSTR are followed meticulously as specified in the academic calendar as approved by the Academic Council. This academic calendar is shared with all the stake holders well before the beginning of the respective academic year. The curriculum and the course contents of all the programmes are discussed by the respective Board of Studies (BoS), analyzed and recommended for implementation. The Academic Council, being the highest statutory body, chaired by the Vice-Chancellor, meets at least twice or thrice a year and discusses, suggests and approves all the important academic matters related to curriculum and course contents in particular including the recommendations of BoS.

The intended revision in regulations (R22) was in principle accepted and recommended by the Academic Council in its 32nd meeting on 10-12-2022. Subsequently respective Board of Studies brought necessary recommendations accordingly, which were duly placed before the Academic Council in its 33rd meeting on 17-6-2023.

1.3 Program Duration

For the branch disciplines listed in section (1), the regular courses including theory and practical are offered over a period of two years in four semesters. The normal duration to complete the M.Tech. program is two years. However, a student can avail the benefit of spill over period for 2 years, that is the maximum duration of four years can be availed by a candidate to complete the M.Tech. programme in a slower pace if he / she desires. The candidate failing to complete the requirements will be considered for the honorable exit as applicable

1.4 Courses and Credits

The term course is used in a broader sense to refer to so called papers such as 'theory subject', 'laboratory', 'inter-departmental project', 'major-project' etc. A course can be of theoretical and / or of practical nature, and certain number of credits are allotted to it depending on the

number of hours of instruction per semester. For a course offered in a semester, one hour of lecture (L) instructions carried out in a week is considered equivalent to one credit, whereas two hours of practical (P) sessions done in a week are considered equivalent to one credit. Depending on the course two hours of tutorial (T) sessions may be considered equivalent to one credit. A student earns these credits when he / she successfully completes the course.

1.4.1 Content Delivery of a Course

Content delivery of a Course in the M.Tech. Degree Program shall be through, either or all, of the following methods:

i. **Lecture** - refers to Lecture Session(s) through classroom contact session wherein students will learn by listening. Denoted by "L".

ii. **Tutorial** - refers to transaction(s) consisting of Participatory discussion / Self-study / Desk work / Brief presentations by students along with such other novel methods that enable a student to efficiently & effectively absorb and assimilate the contents delivered in the lecture sessions. Denoted by "T".

iii. **Practice** - refers to Practice / Practical sessions and it consists of Hands-on- Experience / Laboratory Experiments / Field Studies / Case Studies / Minor / Major Project, that equip the students to acquire the much required skill component. Denoted by "P".

1.5 M.Tech. Degree

All students formally and conventionally enroll for M.Tech. degree programme. They have to earn **68** credits for the award of degree as specified in the Curriculum. However, additionally he/she can opt to earn up to 12 more credits as Add-on credits, to earn the academic benefits as specified below.

1.5.1 M.Tech. with Add-on Certification

If a candidate earns add-on 12 credits in the respective discipline, then he/ she will be eligible for the award of M.Tech. in YY Engineering with Add-on Certification.

Note: The consolidated transcript will contain the credits and grade details of all courses amounting to 68 + up to 12 credits.

1.6 Composition of an Academic year

An academic year is composed of an Odd semester (20 – 22 weeks), an Even semester (20 – 22 weeks) and a Summer semester (6 – 8 weeks). The regular semester that begins in July / August is known as odd / first semester and the one that begins in December / January is known as even / second semester (Figure 1). The instructional days for a regular semester shall be a minimum of 90 working days exclusive of days earmarked for summative assessment.

YEAR OF 12 MONTHS											
1	2	3	4	5	6	7	8	9	10	11	12
July/ Aug.	Aug./ Sept.	Sept./ Oct.	Oct./ Nov.	Nov./ Dec.	Dec./ Jan.	Jan./ Feb.	Feb./ Mar.	Mar./ Apr.	Apr./ May	May/ June	June/ July
ODD SEM/ FIRST SEM					EVEN SEM/ SECOND SEM					SUMMER SEM	

Figure 1: Distribution of semesters during an Academic Year.

1.6.1 Before the commencement of the semester, a candidate has to pay the stipulated tuition fee and submit an application detailing the courses he / she intended to register, valid for that respective Odd / Even semester. The maximum number of credits per semester will be 25 credits inclusive add-on credits. The intended semester wise coverage will be as presented in the curriculum.

1.6.2 **Summer semester** is a short duration semester program that will be generally conducted during the semester break between even semester and odd semester. The students having 'R' (Repeat grade) courses may register for the course work during this semester to get a chance for successfully completing the 'R' courses. In general, supplementary assessments are conducted in the later part of the summer semester. However, the courses offered in summer semester and the number of courses a student can register are subjected to academic and administrative convenience. A student may register up to a max. of 12 credits in a summer semester.

1.6.3 Exception to the routine practice of registering for 'R' courses in summer semester, a student can register in a course offered by a visiting expert during the summer vacation which may be equivalent to a department elective or an Add-on-course. The candidates can register for such courses within the scope of 12 credits. Candidate may also avail summer semester for summer internship opportunities, which may be considered as Add-on credits.

1.7 Semester wise provisions

A student may register for a max of 25 credits per semester as prescribed or otherwise he/she may include the Repeat courses in the event of having not successfully completed a course or courses in the earlier semester. However, a student may also opt to go in a slower pace to earn the credits less than the prescribed max of 25, including even 'Dropping' a semester for special reasons.

It should be clearly underscored that a candidate should on priority register for Repeat (R) credits if any, during a regular semester, within the said scope of 25 credits; in case he / she cannot be sure of completing or could not complete the 'R' credits in Summer semester.

1.7.1 During the first two years from the date of admission to M.Tech., a candidate has to pay the semester / annual fees as prescribed irrespective of the less number of credits that he / she would register or even opt to Drop a semester.

1.7.2 If a candidate gets into spillover semester beyond two years up to a maximum of four years he / she has to pay semester fee proportional to the credits that he/ she registered in that spill over semester as prescribed from time to time.

1.7.3 A candidate has to pay additional fee proportional to the number of credits for registering in a summer semester as prescribed from time to time.

2. CURRICULUM

Each School offers different M.Tech. degree programmes and the departments concerned prescribes semester-wise curriculum encompassing different courses. Every course offered will be designated in a L-T-P structure. The theory courses comprise of L (and / or T & P hours) whereas the practical courses include instructions (T) and practical sessions (P). Amalgamation of theory courses with practical sessions is predominantly seen in this curriculum.

2.1 Distribution of credits

The overall distribution of credits for various categories of courses in the curriculum of M.Tech. programmes is represented in Table (1) as given below.

Table 1 : Credits Distribution for Various categories of courses.

Category of Courses	Credits (%)	AICTE Recommendation (%)
Professional Core	29.4	29.4
Electives	17.6	22.1
Inter disciplinary courses	8.8	7.4
Projects	44.1	41.2

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2.2 Organization of course contents

Courses offered in the program is composed of two modules covering all the course contents required for a candidate to obtain knowledge and skill. Content in each module is further distributed among two units; wherein Unit -1 contains 'Fundamentals and Broad perceptive' of the module. Unit-2 comprises of the extension / advanced topics of Unit-1 as well as necessary practice models for validation / applying the knowledge gained during L/T sessions. The modular period is about 8 weeks. The first unit in a module may be covered in 2 to 3 weeks and the second unit of the module maybe of 5 to 6 weeks (Figure 2). By the end of each module a candidate must be in a position to translate his/ her L-based knowledge into P-based skill as prescribed in the curriculum. Individual formative assessment shall be in place for each module and a single semester-end summative assessment for the course composed of both the modules.

YEAR OF 12 MONTHS											
1	**2**	**3**	**4**	**5**	6	7	8	9	**10**	**11**	**12**
July/ Aug.	Aug./ Sept.	Sept./ Oct.	Oct./ Nov.	Nov./ Dec.	Dec./ Jan.	Jan./ Feb.	Feb./ Mar.	Mar./ Apr.	Apr./ May	May/ June	June/ July
ODD SEM/ FIRST SEM					EVEN SEM/ SECOND SEM					SUMMER SEM	

Module- I		**Module- II**			**Module- I**		**Module- II**			
U1	**U2**	U1	U2		U1	U2	U1	U2		

Figure 2: Unit-wise distribution of course contents in a module and their mapping with Academic Calendar; U= Unit.

3. CHOICE BASED CREDIT SYSTEM

Each branch discipline of the M.Tech. programme comprises of a set of courses - professional core, electives, projects and audit courses. VFSTR offers flexibility for students to choose courses of their choice and obtain the credits satisfying the minimum credits criterion in each category as given in Table-1.

3.1 Professional Core

Professional Core courses are individualized for each programme and they are mandatory for every student opting for that branch discipline. These are designed to offer the essential fundamental knowledge and skills required for that specific programme.

3.2 Electives

A candidate has a choice to choose the elective courses. A list of elective courses are pooled together, enabling a candidate to choose the electives from a pool. There may be more than one pool in certain disciplines aligned to a specific theme. Otherwise also he/ she can exercise the choice to choose electives from across the pools. There may be courses which may not be listed under any pool, which are called 'Free elective courses'.

Elective courses offered for each programme are categorized as 'program electives' that are aimed at offering the advanced/ additional knowledge in the chosen branch discipline.

Care should be exercised while opting for program elective courses and Add-on certification courses that is a course opted as program elective should not be registered as a course under Add-on certification courses and vice versa.

Apart from 68 credits, additionally candidate has to earn 12 credits for Add-on certification. Of these 8 credits may be earned through MOOCs offered via Swayam platform. A student may also be permitted to earn more elective credits through MOOCS. This will promote self-learning and drive students towards innovative learning approaches.

To facilitate the process of acquiring the elective credits through MOOCS, VFSTR has constituted "Online course committee" at Central level with 1-2 members represented from each of the department to guide students in selection of courses and to assist them with further steps if required until completion of the courses.

3.3 Inter disciplinary courses

Courses such as Cyber security, Research Methodology & IPR and employment Orientation/ Soft skills program are offered in the first and second semester of the programme. As per UGC guidelines cyber security course is introduced as compulsory course. The M.Tech. students are encouraged to participate in research activity of both academia and industry, hence research methodology & IPR could be an important course to offer.

The 50-hour Employment Orientation Program (EOP) for M.Tech degree students is conducted with the help of in-house and invited experts. It is aimed at improving presentation skills in general and pedagogical skills in particular.

3.4 Teaching Assistantship

Candidates after undergoing Employment Orientation Programme in the first semester of the program should enroll for the 'Teaching assistantship' course during their second semester to earn 2 credits. Each candidate will assist faculty in handling a 'P-based activities' for B.Tech. students, developing teaching abilities like handling the sessions, interaction with students for clarification of doubts and assessment capabilities. The candidate performance will be assessed in the same lines.

3.5 Inter Departmental Project

These projects are designed and executed by students during the first year second semester of their program. By doing these projects, students will get an idea of how technologies or processes, prototype or working model can be developed by culmination of technologies from courses of different programs. The minimum duration of inter-departmental project during each of the semester is 90 hours including writing of project report and submission for assessment. A batch of 2-3 students from same or across the departments can take part in each of the inter-departmental projects. Performance will also be assessed in the modular framework for formative and semester-end summative with a weightage of 2 credits

3.6 Project

Students may opt for Project work in lieu of internship for two complete semesters during second year. Such students may avail research-internship support from any institution well known for research and development (R&D). They may also take up project work in VFSTR itself. Each candidate has to submit interim reports and a final report which are mandatory requirements towards the partial fulfillment of project credits requirements. It bears a weightage of 13 credits for the work executed in the third and fourth semesters totalling up to 26 credits. During the project work the student under the guidance of a faculty member(s) will involve in an innovative design / research through the application of his / her knowledge gained in various courses studied. He / she is therefore expected to present a survey of literature on the topic, work out a project plan and carry it out through experimentation / modelling / simulation / computation. Through such a project work, the student is expected to demonstrate system analysis, design, presentation and execution skills. Performance in the project will also be assessed in the modular framework for formative and summative assessments.

3.7 Internship

A student can undertake internship in lieu of project work in industry for two complete semesters during second year in lieu of major project work. It bears a weightage of 13 credits for the work executed in the third and fourth semesters totalling up to 26 credits. This is aimed at training students in solving / understanding real-life problems through application of engineering analysis, design, evaluation and creation, particularly in association with practitioners and experts in the industry. The procedures for obtaining the internship placements and allocation of the same to the students are as per University. Even during internship, a student is preferably expected to carry out a focused study on one topic / problem in consultation with the interning institute. Internship progress report should be submitted periodically and finally a detailed internship report should be submitted duly certified by a mentor from the internship institute. Performance in the internship will also be assessed in the modular framework for formative and summative assessments.

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4. ATTENDANCE

It is mandatory for the student to attend the course work in each semester as per the academic schedule of that semester. VFSTR expects 100% attendance. However, the attendance in each course shall not be less than 75 % of the aggregate of all L, T, P sessions conducted in that course.

a) The attendance calculations will be periodically reviewed at the end of every 4 weeks. The details of attendance status will be shared with the parents / guardian. The final status of attendance will be reported at end of 15th week granting the advantage of the attendance for the 16th week for the purpose of attendance shortage calculations.

b) The shortage of attendance may be condoned up to 10% on the ground of ill-health, social obligations, participating / representing in sports/cultural events, placement activities etc.

c) Documentary evidence like medical reports and certificates issued by concerned bodies is to be produced on time as support for the attendance shortage due to ill-health. These cases are subjected to the scrutiny of a committee constituted for this purpose by the Vice-Chancellor. The decision of the committee shall be final.

d) Prior approval has to be taken from the HoDs for the other types of leaves.

e) The courses where the student shortage of attendance was not condoned shall be considered as 'Repeat' category courses and will be under 'R' grade in the student's semester transcript. Student should re-register for these courses during the summer semester or whenever the course is offered next time during regular semesters. These re-registrations are subjected to the regulations at the time of re-registration. In case of core courses, the same core has got to be re-registered. However, in case of an elective a candidate may exercise a choice of choosing different elective in place of 'R' graded elective.

The students who are put into 'R' grade will not be allowed to take up the summative assessment in that semester. In case due to lack and/or delay in information, if he/she appears for the summative assessment in that course, office of AAA is empowered to cancel the attended exams. The scores obtained either in formative or summative assessment will not be considered for grading.

5. ASSESSMENT

Teaching-Learning and Assessment should go hand in hand and complement each other. Continuous assessment plays a vital role to enable the student to get synchronized with the teaching-learning process. Assessment mechanism adopted in the institute is aimed at testing the learning outcomes in tune with the outcome based model of education. The focus, is thus on assessing whether the outcomes are realized by the end of the course.

The performance of a student in each course is assessed on a continuous basis during the semester through various in-semester and end-semester assessment models. The marks awarded through continuous assessment are referred to as Formative assessment marks. The marks awarded through end-semester tests are referred to as Summative assessment marks (Figure 3). Both the formative and summative assessment marks are considered for awarding the final marks and the grade point in a particular course.

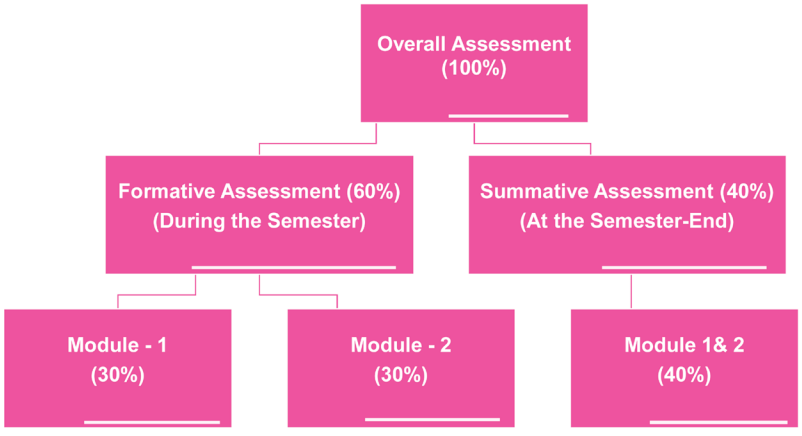

Figure 3: Categories of assessments in place for R22.

5.1 Marks distribution

For each course, the maximum sum of formative and summative assessment marks put together is 100, in the ratio of 60:40, respectively.

5.2 Qualifying criteria

To be declared successful in a course, a student must secure at least a grade 4.5 in a scale of 10 based on the total maximum marks which is inclusive of formative and summative assessment. The students should also get 40% from the maximum marks allotted for formative and summative assessments individually.

The hierarchy of qualifying criteria is as follows:

i. Attendance compliance should be 75% or within condonable range; else the candidate is put into 'R' grade.

ii. In formative assessment, a candidate should secure a minimum of 40% i.e. 24 marks out of 60; else the candidate is put into 'R' grade.

iii. In summative assessment, a candidate should secure a minimum of 40% i.e. 16 marks out of 40; else the candidate is put into 'I' (Incomplete) grade.

iv. Collectively the candidate should secure a min. grade of 4.5 in a scale of 10 after relative grading; else the candidate has to choose either 'R' or 'I' grade duly being counselled.

v. Every semester, candidate should score a min. of 5 Semester Grade Point Average (SGPA) in every semester individually with the successfully completed courses. In case a candidate fails to score the min. SGPA, then he / she shall voluntarily drop a few Courses to ensure a SGPA of 5. He / she after duly counselled has to choose either 'R' or 'I' grade for the dropped courses.

The candidates with 'R' grade should re-register for 'R' courses either in Summer semester or in a regular semester as and when the courses are offered. The candidates in 'I' grade are allowed to appear for supplementary summative assessment whenever the semester-end assessments are conducted.

To assess special projects / courses, not fitting into the categories described here, a suitable assessment procedure will be evolved in consultation with experts of that area and adjudicated by the committee constituted for that purpose. The decision given by the committee will be final. The appended assessment scheme shall be announced by the course coordinator during the commencement of course.

YEAR OF 12 MONTHS											
1	**2**	**3**	**4**	**5**	6	7	8	9	**10**	**11**	**12**
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ODD SEM/ FIRST SEM					EVEN SEM/ SECOND SEM					SUMMER SEM	

Module- I		**Module- II**			**Module- I**		**Module- II**			
U1	**U2**	**U1**	**U2**		**U1**	**U2**	**U1**	**U2**		
Formative Assessment				SA	Formative Assessment				SA	

Figure 4: Schedules of formative and summative assessments in line with Academic calendar. SA = Summative assessment.

5.3 L-based courses integrated with P/T

5.3.1 Formative Assessment

The scheme of formative assessment is designed to promote the continuous learning. Scheme consists of assessments planned at institute level and assessment that may be scheduled by

the course instructor (Figure 4). Institute level assessments shall be scheduled by the office of AAA. Respective Faculty Member(s) shall declare the schedule of Continuous Laboratory Assessments (CLA), Quiz, Tutorials, Assignments, Seminars, Discussions, etc. Some of the components may also however take place in an unscheduled manner like Surprise Tests. However, students shall be made aware of the assessment modalities that are going to be followed in a course by the faculty, under information to the HoD.

To monitor the progress of students, continuous assessment comprising of five targets (T1, T2, T3, T4 and T5) is advocated in each module for a maximum of 60 marks. For a class, formative assessment commences by the announcement of module bank containing 10 problems for each module in a course. Nature of problems in the module bank shall be at the level of creative / exploratory / design / thought provoking covering the complete syllabus of a module at advanced / challenging level.

The purpose of creating module bank of 10 problems is to assign one problem to each student or to a batches of 2 members. The batches are composed of randomly picked up candidates. These batches remain same for all courses and also for the P-sessions in the courses in that semester and are created in the beginning of that semester.

The purpose of assigning one problem to two batches is to create a healthy competitive spirit between the two batches.

The modality of evaluation of five targets is listed here under:

a) **T1**: During 5th or 6th week of each module a classroom test shall be conducted. T1 consists of two parts: A and B.

Part A consists of one random problem from the module bank and varies from batch to batch. All the questions in the module bank shall be distributed among students and students shall know the question to be answered only on the day of test in the examination hall.

Part B consists of one common problem at fairly application/ advanced level **(not at all prior notified)** from outside the module bank for all the students.

T1 shall be paper based and proctored test for a period of 60 min (maximum) which shall be assessed for 30 marks and downscaled to 10 marks.

For the students who for justifiable reasons could not attend the classroom test on the scheduled day, a re-test maybe conducted. However, Part-B will contain a new question and Part-B will have higher weightage than part-A or full weightage could even be allotted for Part-B in such an event

b) **T2**: Immediately follows T1. Students in a specified batch who now have received the same question during T1 will work further on that problem for T2.

T2 is primarily an extension of problem received in T1 for carrying out validation study: Case studies / Simulations / Experimentation. Each batch shall interact with the course instructor to finalize the nature of validation and expected to complete the exercise within 10 to 15 days after T1.

Course instructor should ensure assigning a different case study / a different scope for validation study for each batch in case the same problem is assigned to two batches.

Course instructor shall assess every student in a batch for a max. of 10 marks based on his observation, interaction and/or reviewing (based on at least two reviews).

c) **T3**: T3 shall be conducted during the last week of each module. Student batches are expected to submit a report, clearly documenting the work executed during T2. The report should be in IEEE / APA format and additionally a voice in-built PPT should be prepared and submitted.

The report and presentation shall be assessed by the course instructor for 10 marks for every student. In certain cases, a course instructor can call a batch for a physical presentation also.

d) **T4**: T4 is a comprehensive module test, conducted for 30 min. comprising of 20 multiple choice questions (MCQs) covering the holistic content of module. T4 shall be evaluated for a max. of 10 marks @ ½ mark for each question. T4 will be conducted in ON-LINE mode.

There shall be two tests in each course in a day and the best performance of the tests shall be considered for awarding the marks.

Two sets of question papers each containing 20 questions should be set. The theme of the questions could be similar across the sets. When the test is administered online, every student receives the questions in shuffled sequence and also the choices in shuffled sequence. Therefore, the choice like both 'a' & 'b' above, neither 'a' nor 'b', all the three a, b, c will not be set.

e) **T5:** T5 assessment is based on Practice or Tutorial assignments. Implementation, Report presentation and Discussion shall happen in a continuous mode throughout the module period.

At least 4 such continuous lab practice assessments (CLPA) / assignments per module shall be conducted by course instructor. The marks will be @ 5 marks per assignment totalling up to 20 per module.

f) The scores of the targets are to be normally announced within three working days on completion of the assessment and the performance is to be discussed in the class.

g) The total marks per module is 60 - T1 (out of 10), T2 (out of 10), T3 (out of 10), T4 (out of 10) and T5 (out of 20).

h) Total marks for both the modules from formative assessment will be added up to 120, which will be ***suitably mapped down*** to a max. of 60 marks. The mapping policy should be decided by the lead instructor / instructors in consultation with the HoD. The mapping policy should be shared with Dean AAA for the purpose of documentation.

i) The marks scored in Module-1 for a max. of 60 should be entered / submitted latest by 9th week and of Module-2 latest by 17th week of the semester. Consolidated score for a max. of 120 ***suitably mapped down*** to a max. of 60 marks should be submitted latest by 18th week of semester enabling the declaration of 'R'- grade before the commencement of summative assessment.

j) A candidate put under 'R'- grade will not be permitted to take up the summative assessment.

5.3.2 Summative Assessment

a) An instructor may choose one of the two formats for conducting summative assessment for L-based courses integrated with T/P.

i) 15 + 25 marks format or 20 + 20 marks format (following b, c, d below).
ii) 40 marks format (following c, d below).

b) **If summative assessment is in two parts format:**

i) Part-I will be the assessment of capstone project which is pre-assigned during the module-2 period or will be the exploratory review assessment of all lab practice assignments.

ii) Part-II will be based on a written examination for a max. marks of 80, as in c & d below, which is ***scaled down*** to 25 or 20 based on the selected pattern of format.

iii) A candidate should attend both the parts of summative assessments; else he will be put into 'I' grade.

c) For each L-based course integrated with T/P, the summative assessment shall be conducted by the Institute for a duration of 150 min. and for a maximum of 80 marks. Contents for summative assessment shall cover the breadth and depth of the complete syllabus that is mentioned in the two modules of a course.

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d) The question paper for end-semester theory examination consists of two parts as given in Table (2).

Table 2: L-based Summative Assessment Question Paper Pattern.

Part No.	No. of Questions	Marks for each Question	Marks	Choice
A	4	10	40	No
B	2	20	40	No
Total Marks			80	

e) The questions will be comprehensive covering the entire course syllabus and any single question should not necessarily be limited to any particular unit / module.

f) These marks are ***suitably mapped down*** to a score of 40.

g) Total marks of summative assessment will be for a max. of 40 irrespective of format of evaluation.

h) The award of 'I' grade is solely based on marks scored in summative assessment out of 40, if he/she does not score a min. 16 out of 40 (40%).

5.4 P-based Courses

The detailed information consisting of experiments, batch formations, experiment schedules, etc., will be displayed / informed to the student in the first week of the semester so that the student comes prepared for the lab sessions. Copies of the manual will be made available to the students along with the schedule. The manual will consist of the list of equipments, detailed procedure to conduct the experiment, format for record writing, outcomes for each experiment and possible set of short questions to help students gain critical understanding. The courses like Cyber security, Research Methodology & IPR will also be treated as P-based courses.

5.4.1 Formative Assessment

During practice sessions, a brief viva-voce is conducted for each student on the experiment he/she is carrying out on that day. Some of the parameters that could be included in the Continuous Practice Assessment (CPA) are given in Table (3). The set of parameters may slightly differ from one laboratory to the other, and will be announced before the commencement of the practice session. These parameters are assessed for each laboratory session.

Table 3: Suggested parameters for Continuous Practice Assessment (CPA).

S. No	Component	Marks
1	Report of about 1 page on proposed experimental layout and background theory before the start of lab session	4
2	Viva and interaction to evaluate understanding of concepts	4
3	Experimentation and data collection	4
4	Analysis of experimental data and interpretation	4
5	Finalized report submitted in the next week	4
Total		**20**

This assessment is carried out for each practical session and the total marks of all practical sessions will be ***suitably mapped down*** to a max. of 60.

5.4.2 Summative Assessment

End semester examination for each practical course is conducted jointly by two examiners. The examiners are appointed by Dean, AAA from the panel of examiners suggested by the respective Heads of the Department. In some cases, one of the examiner may be from outside the institution and will be identified as external examiner. The scheme of assessment may vary depending on the nature of laboratory, which shall be shared with student by the

laboratory in-charge. The summative assessment will be conducted for a max. marks of 40. The general scheme of assessment is given in Table (4).

Table 4: Suggested end-semester summative assessment pattern for P-based courses.

Component	Marks		
	Examiner 1	Examiner 2	Total
Objective & Procedure write up including outcomes	4	4	08
Experimentation and data collection	4	4	08
Computation of results	4	4	08
Analysis of results and Interpretation	4	4	08
Viva Voce	0	8	08
Total Marks	16	24	40

5.5 Assessment and Grading of MOOCs based elective

Whenever a candidate opts for a course through MOOCS offered via Swayam platform, he / she has to learn and undergo assessment as per norms set by VFSTR for such MOOCs Courses. Upon the declaration of the result, that the candidate has successfully completed the course, the candidate is said to have earned the credits under credit equivalence and credit transfer.

5.6 Inter Departmental Project

Inter departmental project work is undertaken in the 2nd semester for earning 2 credits by each candidate. It is expected that the inter- departmental Projects result in publication of a technical paper in a peer-reviewed journal. For this purpose, Dean R&D and Heads of Department will identify faculty mentors who will guide the students by conducting workshops on drafting of research article, communication, process of peer-review, publication, etc. The faculty will support the students by all means to get the technical findings published in peer-reviewed journals.

5.6.1 Formative Assessment

The assessment will be carried in two reviews in a systematic way. The detailed assessment guidelines and scheme are to be announced along with the assessment schedule as mentioned in the Table (5).

Table 5: Schedule and parameters followed for formative assessment.

No of Module	Schedule	No of reviews	Points to be considered	Formative assessment marks
Module -1	7th – 8th week	Review -1	• Identification of specific area out of broad areas under the supervisor • Identification of outcomes in line with programme objectives. • Feasibility of contributing to the attainment of outcomes • Identification of tools / equipment / surveys / training needs / etc..	30
Module – 2	15th–16th week	Review -2	• Presentation of results, analysis and conclusions • Meeting of objectives defined in first review • Preparation of report • Understanding by individual students on the overall project • Submission of technical article	30

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5.6.2 Summative Assessment

Summative assessment will be done jointly by two examiners. The examiners are appointed by Dean, AAA from the panel of examiners suggested by the respective Head of the Departments. In some cases, one of the examiner may be from outside the institution and will be identified as external examiner. The scheme of assessment will be report (15 marks), presentation (10 marks) and demonstration (15 marks) respectively. Points to be considered during the review.

a) Presentation of results, analysis and conclusions
b) Meeting of objectives defined in first review
c) Preparation of report
d) Understanding by individual students on the overall project
e) Individual student contribution
f) Progress of project as per schedule
g) Submission of technical article/ prototype realization

5.7 Project

Those students who do not opt for the internship, carry out their major project at VFSTR and submit their report which is a mandatory requirement for the award of degree. These projects are usually done individually during third and fourth semesters, under the guidance of a faculty member. Every candidate, in consultation with the guide, should define the project and also the probable procedure of carrying it out and submit the same to a committee consisting of 2 to 3 faculty members appointed by Head of the Department. This is to avoid the repetition and also to come up with a roadmap for completion of the project within the time stipulated. The students are encouraged to select topics related to ongoing research and consultancy projects. The students are expected to carry out and present a survey of literature on the topic, work out a project plan and its implementation through experimentation / modelling / simulation / computation. They are also expected to exhibit system analysis, design, and presentation and evaluation skills.

5.7.1 Formative Assessment

The progress of project is reviewed twice in a semester by the Project Review Committee (PRC) and formative assessment marks are awarded based on these reviews. The Project review committee consists of

a) Head of Department or his/her nominee – Chairperson
b) A senior faculty member identified by the HoD – member
c) Project supervisor – member

Review schedules of PRC are to be announced by the department immediately after the commencement of semester. The review presentations are open to all the students of that section and attendance is compulsory. The first review should be of 15 minutes / student; second review should be around 30 minutes / student. Before every review every student should submit their PPT along with a brief report of not exceeding two pages. It is to be expected by the committee that student communicates / publishes research article based on the project work prior to graduation either in a peer-reviewed journal or top-notch conference. Based on the recommendations of the committee, he / she is expected to continue same research problem in the third and fourth semesters to derive possible solutions. The following aspects may be considered by the committee for assessment Table (6).

Table 6: Schedule and suggested parameters to be considered for formative assessment.

Semester	Module	Schedule	Review	Points to be considered	Max. Marks
Semester III	Module -1	7th – 8th Week	First review	• Identification of specific area out of broad areas. • Identification of outcomes in line with programme objectives • Feasibility of contributing to the attainment of outcomes	20
	Module -2	15th – 16th Week	Second review	• Identification of tools / equipment / training needs / etc. • Understanding by individual students on the overall aspect of the project • Completion of literature survey • Design of project set up	40
Semester IV	Module -1	7th – 8th Week	First review	• Acquisition / learning of the tool required • Readiness of the layout of the project report • Progress review as per mechanism / schedule identified • Preparation of draft manuscript for publication	20
	Module -2	15th – 16th Week	Second review	• Presentation of results and conclusions • Meeting of objectives defined in first review • Submission of draft report • Understanding by individual students on the overall project • Progress of project as per schedule • Progress of the publication	40

5.7.2 Summative Assessment

At the end of III & IV semesters, summative assessment of the project will be conducted in two phases.

Phase–I: This is an evaluation for a max of 20 marks. A committee of two members comprising of HoD's nominee and Guide will assess the project work which will involve going through the project report (6 marks), project presentation (7 marks) and demonstration of the project (7 marks).

Phase–II: A final presentation and defense assessment for a max. of 20 marks will be carried out by one-man committee composed of an external expert who is chosen by the Dean AAA from a panel of examiners suggested by the HoD. The format for evaluation will involve going through the project report's quality (6 marks), presentation (6 marks) and interaction and defense (8 marks).

The qualifying marks will be finalized considering the marks scored in both the phases (I & II) of summative assessment.

Publication in a top-notch conference / peer-reviewed journal is mandatory for evaluating the project for 100% weightage.

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In case the candidate is placed in 'I' grade, he/she has to appear for both Phase-I and Phase-II assessments, which will be held within the 15 days after declaration of results. In the consecutive assessment also if the candidate fails to secure min. required score, then he / she will be placed in 'R' grade.

5.8 Internship

Internship work is undertaken by a student in an industry, under the joint supervision of industry personnel and an internal faculty member. Sixty percentage of the marks of Internship are allotted through continuous evaluation as formative assessment and the remaining 40% are based on summative assessment.

Table 7: Assessment scheme for Internship reviews.

Semester	Module	Schedule	Review	Formative assessment marks
Semester III	Module -1	7th – 8th Week	First review	20
	Module - 2	15th – 16th Week	Second review	40
Semester IV	Module - 1	7th – 8th Week	First review	20
	Module - 2	15th – 16th Week	Second review	40

a) The progress of internship work is reviewed twice in every semester by the "Internship Review- Committee (IRC)" and marks for formative assessment are awarded based on these reviews.

b) The IRC consists of Head of Department or his/her nominee (Chairperson), the internal and external (industry) supervisors.

c) The IRC may not be the same for all students; however, the same IRC should exist for entire duration of the internship program of any single student.

d) The schedule and the scheme of evaluation are to be announced with internship notification. The internship reviews may take place at the place of internship or at the university, as decided by the interning organization or may be conducted in the blended mode.

5.8.1 Formative assessment: Internal reviews at the place of internship

The internal supervisor will interact with the guide allotted at internship offering industry based on the schedule given to conduct the reviews. Scheduled reviews can be conducted by IRC on online mode for discussion/ presentation. The marks shall be distributed for each student in the scheduled reviews as given in Table (7).

a) Students should submit a report (not more than two pages) explaining about the progress of their work, mentioning clearly details like the machines or software handled / adopted, type of data collected and his/her understanding and contribution in the programme, and the same has to be presented before the supervisors.

b) The candidate should clearly present the completion of stipulated assignments set by the industry supervisor for that period.

c) The evaluation will be based on a & b above and also based on regularity and discipline maintained in the internship venue.

Table 8: Suggested scheme of assessment for every review

Component	First review	Second review
Regularity and interaction	5	10
Application of knowledge	3	6
Gaining of new knowledge /skills / literature survey	3	6
Internship progress	5	10
Report	4	8
Total marks	**20**	**40**

5.8.2 Summative assessment – Internship

At the end of III and IV semesters, the student shall submit a comprehensive report of internship covering the work done and make a final presentation in two phases as follows:

Phase–I: A committee of two members comprising of internal supervisor and HoD's nominee will assess the overall internship participation by the candidate and his final report through presentation made by the intern. The internship report (6 marks), presentation (7 marks) and overall impression (7 marks) during the internship will be evaluated respectively.

Phase–II: A final presentation and defense assessment for a max. of 20 marks will be carried out by one-man committee composed of an external expert who is chosen by the Dean AAA from a panel of examiners suggested by the HoD. The format for evaluation will involve going through the project report's quality (6 marks), presentation (6 marks) and interaction and defense (8 marks).

The qualifying marks will be finalized considering the marks scored in both the phases (I & II) of summative assessment.

Publication in a top-notch conference / peer-reviewed journal is mandatory for evaluating the Internship for 100% weightage.

In case the candidate is placed in 'I' grade, he / she has to appear for both Phase-I and Phase-II assessments, which will be held within the 15 days after declaration of results. In the consecutive assessment also if the candidate fails to secure min. required score, then he / she will be placed in 'R' grade.

6. SEMESTER-END ASSESSMENT ACTIVITIES

6.1 Setting of semester-end summative assessment question papers will be coordinated by the instructor assigned for a particular course. Two sets of question papers will be submitted latest by 12th week of the semester.

6.2 There shall be 'Summative Assessment Question Paper Scrutiny Committee' which would be constituted with external experts. Experts are empowered to modify / rephrase the questions to maintain a high standard of the semester-end assessment. The review should be completed by the 14th week of the semester. The review process will be coordinated by a committee of School Dean, HoDs and external experts.

6.3 The question wise marks scored in the summative assessment out of a total of 80 will be made available online within two weeks from the last date of examination and would be kept active for 24 hours. Latest by the end of 48 hours from the instant of notification any candidate can submit an appeal online providing question wise claim.

6.4 Claims for re-assessment on P-based courses are not allowed.

6.5 The appeals will be attended within next three working days. Fees for appeal, as decided from time to time, has to be remitted online along with the appeal.

6.6 Final results and grades will be computed as explained in the next section.

6.7 Final results and grades shall be announced within four weeks of completion of the last examination of the summative assessment (within two weeks from the last date of appeal). Grades are published on the University website, and also informed to the parents and students through SMS.

6.8 Provisional Grade cards will be issued within two weeks after the announcement of grades. Grade card will contain three parts. Part 1: Details of successfully completed courses. Part 2: Details of 'I' grade courses. Part 3: Details of 'R' grade courses.

7 COMPUTATION OF GRADING

7.1 Formative assessment decides the list of 'R'- candidates. Therefore, these candidates will not be considered for grading computation. Summative assessments decide the list of 'I' candidates. Therefore, these candidates will not be considered for grading computation.

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7.2 The candidates who have successfully completed both formative and summative assessments will be considered for computation of relative grading.

7.3 Threshold value (**Th**) for relative grading in each course is arrived after studying the marks distribution in that course by a committee constituted by office of Dean AAA. The threshold value is decided by the upper bound marks of the major chunk of the class keeping the top outlier scores away from consideration (the least upper bound). The threshold value will be slightly greater than upper bound marks or may be equal to the upper bound marks.

7.4 The total marks (**m**) = marks scored in the formative assessment + marks scored in the summative assessment is transformed into relative grade expressed accurate to two decimal places as follows:

Relative grade point (P) = (m/Th) X 10 [and limited to 10]

7.5 If students require course wise percentage equivalence, then the calculation will be based on the following

Course wise percentage equivalence = (m/Th) X100
[truncated to two-digit integer and limited to 100]

7.6 After relative grading, a student is assigned a 'Letter Grade (G)' for each course as per Table (9). The grade and the corresponding letter grade represent the outcomes and assessments of a student's performance in a course.

Table 9: Grading information

Relative Grading Range (P)	Category	Grade (G)
≥ 9.50	Outstanding	O
≥ 8.50 to 9.49	Excellent	S
≥ 7.00 to 8.49	Very good	A
≥ 6.00 to 6.99	Good	B
≥ 5.00 to 5.99	Fair	C
≥ 4.50 to 4.99	Marginal	M
Transitional Grade	Repeat	R
Transitional Grade	Incomplete	I

8. SUPPLEMENTARY EXAMINATIONS

8.1 The supplementary examinations shall be conducted once in summer semester. Notifications will be released by the AAA section informing the students about registration procedures, details of fee and timetables. Apart from these examinations the students who have courses with 'I'-grade can also write the supplementary examinations along with regular semester-end examinations of that academic (Odd / Even) semester.

8.2 Whenever a candidate clears courses with 'I' grade in a supplementary examination that are conducted during a regular semester, the Threshold value for computing his / her grade will be obtained from the same batch in which he / she had completed his / her formative assessment.

8.3 Whenever a candidate clears courses with 'R' / 'I' grade in a summer semester, the Threshold value for computing his / her grade will be carry forwarded from the preceding Odd / Even semester for the respective courses.

8.4 Whenever a candidate clears courses with a 'R' grade in a regular semester along with his/ her junior batch then for this candidate the Threshold value will be corresponding to his/her junior batch for computing grade.

8.5 The results of summative assessment of Project / Internship will be announced only if the candidate successfully earn all the credits in courses registered during the program. If the candidate is with 'R' / 'I' graded courses the results will be kept under **'Announced Later (L)'** status and will be announced only after candidate clears these courses.

9. GRADE POINT AVERAGE

The Academic Performance of a student in every semester is indicated by the Semester Grade Point Average (SGPA) and finally by Cumulative Grade Point Average (CGPA).

9.1 SGPA

The Semester Grade Point Average (SGPA) shall be computed using the formula given below:

$$SGPA = \frac{\sum_{i=1}^{n} C_i P_i}{\sum_{i=1}^{n} C_i}$$

Where

n = number of courses a student successfully completed in the semester under consideration

Pi = Grade points secured for the i^{th} course registered in the semester under consideration.

Ci = the number of credits assigned to i^{th} course registered in the semester under consideration.

9.2 CGPA

The Cumulative Grade Point Average (CGPA) shall be computed after successful completion of the programme. The CGPA shall be expressed in different flavors to reflect M.Tech. of 68 credits, and Add-on certification up to 12 credits.

Accordingly, the computations will be as below:

$$\text{CGPA} = \frac{\sum_{j=1}^{m} C_j P_j}{\sum_{j=1}^{m} C_j}$$

Where

m = total number of courses prescribed for the completion of the programme

Pj = grade points secured for the j^{th} course.

Cj = the number of credits assigned to j^{th} course

and Σ Cj = 68

Σ Cj = 08 for CGPA calculations in case of M.Tech. with Add-on certification

Σ Cj = 12 for CGPA calculations of specialization part in case of M.Tech. with Add-on certification

Percentage equivalence of SGPA & CGPA = (SGPA or CGPA) X10

10. AWARD OF CLASS

The students who have become eligible for award of degree shall be classified based on their CGPA secured, as per the Table (10) given below:

Table 10 : Class/ Division information.

Sl. No.	CGPA	Class / Division
1	8.0 and above	First Class with Distinction
2	6.5 and above but less than 8.0	First Class
3	6.0 and above but less than 6.5	Second Class
4	Less than 6.0	Pass Class

a) For the purpose of rewarding the accomplishers with ranks and awards, toppers in each branch discipline are identified, based on their academic performance (CGPA) in the following categories:

i) Ranking in M.Tech.

ii) Ranking in M.Tech. with Add-on certification

b) In addition, the 'Chairman's gold medal' and other 'Endowment Awards' are awarded to

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the 'outstanding students' based on the overall performance which includes academic, co-curricular and extra-curricular activities, campus placements and competitive examinations. A committee appointed by the Vice-Chancellor will recommend the eligible student for the award, selected from the nominations received from the departments.

c) In addition, the institution may recognize exceptional performance such as music, dance, sports etc. and display of exceptional bravery from time to time.

d) Only such candidates who complete 68 credits (+12 credits) in the first 4 successive semesters shall be eligible to receive awards/ ranks.

e) The candidates availing spill over semesters will not be eligible for the award of merit scholarships.

11. AWARD OF DEGREE

On successful completion of prescribed requirements of the programme, the degree shall be conferred during the convocation of the VFSTR.

For the conferment of degree, the student has to fulfill the following requirements:

a) a bonafide student and undergone the course work of not less than two academic years and not more than four academic years from the date of joining.

b) successfully completed all the courses as prescribed in the respective curriculum.

c) acquired a minimum eligible credits i.e. 68 credits for the award of M.Tech. degree.

d) obtained no due certificates as prescribed by VFSTR.

e) no in-disciplinary proceedings pending against him / her.

Consequent upon being convinced, following an enquiry, the Academic council may resolve to withdraw the degree / diploma / any other certification provided by the institute. The aggrieved may however prefer for a review of such decision by the Academic Council, citing cogent reasons for review or go in for an appeal to the, BoM of the institute.

12. Honorable exit with Engineering PG Diploma

In line with NEP-2020, an optional exit is provided for a candidate who has earned a min. of 40 credits and has completed all the requirements up to the end of two semesters.

Engineering PG Diploma will be awarded in respective branches of specialization. In case the candidate fails to earn 40 credits, a suitable certification will be awarded during his / her exit from M.Tech. degree.

Semester-wise transcript and a consolidated transcript will be given to the candidates during their exit from the registered program.

Such a candidate who has exited can seek re-entry to complete M.Tech. by surrendering the Engineering PG Diploma. A committee constituted by Vice-Chancellor will scrutiny all such re-entry requests and recommend the plan of action. However, the max. duration of programme should be limited to four years and further extension beyond the stipulated max. duration of study has to be approved by Academic Council, if the candidate appeals for an extension.

13. Onward Continuation to Ph.D. Program

As per the section 6.2 of R-22 Ph.D. regulations, candidates pursuing M.Tech. at VFSTR, who have completed all the courses prescribed for the first 2 semesters with a minimum of 60% or equivalent CGPA may be considered for onward continuation to Ph.D. program with a provisional admission to Ph.D.

For such candidates, a faculty mentor is allocated after the provisional admission. Mentor could become a Research Supervisor for the Ph.D program after confirmation of Ph.D admission at VFSTR, which is after formally completing M.Tech degree requirements.

Candidate in consultation with the faculty mentor shall identify the broad area of research topic and can utilize the M.Tech Project as a preliminary work before commencing the intensive research work during Ph.D programme. The M.Tech project work under the guidance of faculty mentor should satisfy all the mandates prescribed in the regulations of M.Tech. However, candidate is required to hold a Master's degree in Engineering / Technology with a minimum of 60% or equivalent CGPA before being formally admitted into the Ph.D program

14. Volunteer 'Drop' with Sabbatical Semester option

A candidate may exercise his option to voluntarily exit from M.Tech. programme temporarily for a semester during the M.Tech. programme, by registering for a 'DROP option' in the beginning of the semester after completion of first two semesters. The DROP can be exercised to take up special Internship / Innovation / Exploratory / Entrepreneurship / Advanced research / Start-up and such related activities. Under such circumstances a candidate can normally avail DROP over two successive semesters. Such 'Drop' semester will be identified as Sabbatical semesters.

Such a candidate has to pay the regular semester fee if such a Drop option is utilized during the first 4 semesters of M.Tech., and has to pay a nominal semester maintenance fee during the spillover period, if a candidate has not yet completed the credit requirements.

Upon returning from such a temporary exit, a candidate may continue his M.Tech. studies utilizing the provision of spillover period. A candidate may also submit a claim for Credit equivalence for the activities undertaken during the sabbatical period. The equivalence committee would evaluate and assess the academic equivalence of the work carried out and would recommend the credit equivalence and credit transfer to be granted together with the grades that could be attributed, if applicable. However, the max. duration of programme should be limited to four years and further extension beyond the stipulated max. duration of study has to be approved by Academic Council, if the candidate appeals for an extension.

14.1 Volunteer 'Drop' with Semester Drop option

A candidate may exercise his option to voluntarily exit from M.Tech. programme temporarily for a semester during the M.Tech. programme, by registering for a 'DROP option' in the beginning of the semester to meet the family / personal exigencies. All the norms as mentioned in the section (14) shall be applicable for the candidates utilizing semester drop option.

15. INTERPRETATION OF RULES

a. The academic rules and regulations should be read as a whole for the purpose of any interpretation.

b. For the matter(s) NOT covered herein above or for unforeseen circumstances, but arising during the course of the implementation of the above regulations. The Vice-Chancellor shall be authorized to remove the difficulties and decide upon the matters. The same shall be reported in the next meeting of Academic Council for ratification and subsequently informed to BoM.

c. The Institution may change or amend the academic rules and regulations or curriculum at any time, and the changes or amendments made shall be applicable to all the students with effect from the dates, notified by the Institution.

d. Procedure and explanation to any section can be floated by the office of Dean AAA as applicable from time to time with due approval by the chairman of Academic Council.

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R22 - M.Tech. - Course structure

I Year I Semester

Course Code	Course Title	L	T	P	C
	Professional Core - 1	2	2	2	4
	Professional Core – 2	2	2	2	4
	Professional Core – 3	2	2	2	4
	Department Elective – 1	2	-	2	3
	Department Elective – 2	2	-	2	3
	Cyber security	1	2	-	2
	Employment Orientation Program	-	2	2	2
Total		**11**	**10**	**12**	**22**
		33 Hrs			

I Year II Semester

Course Code	Course Title	L	T	P	C
	Professional Core – 4	2	2	2	4
	Professional Core – 5	2	2	2	4
	Department Elective – 3	2	-	2	3
	Department Elective – 4	2	-	2	3
	Research Methodology & IPR	1	2		2
	Inter Departmental project	-	1	3	2
	Teaching assistantship	-	-	4	2
Total					20
	Add-on certification course -1	3	-	2	4
Total		11	7	17	24
		35 Hrs			

II Year I Semester

Course Code	Course Title	L	T	P	C
	Project / Internship	-	2	24	13
	Add-on certification course -2 (MOOCs / Self-Study Course)	4	-	-	4
Grand Total		**4**	**2**	**24**	**17**

II Year II Semester

Course Code	Course Title	L	T	P	C
	Project / Internship	-	2	24	13
	Add-on certification course -3 (MOOCs/ Self-Study Course)	4	-	-	4
Grand Total		**4**	**2**	**24**	**17**

M.Tech VLSI Design

R22 Corse structure and Syllabus

I Year I Semester

S.No	Course Code	Course Type	Course Title	L	T	P	C
1.	22VLB101	Professional Core -1	Semiconductor Device Modeling	3	-	2	4
2.	22VLB102	Professional Core -2	Analog IC Design	3	-	2	4
3.	22VLB103	Professional Core -3	Digital IC Design	3	-	2	4
4.		Department Elective -1	-	2	-	2	3
5.		Department Elective -2	-	2	-	2	3
6.	22CYB101	Cyber Security	Cyber Security	-	2	2	2
7.	22SAB101	EOP	EOP	-	2	2	2
Grand Total				13	4	14	**22**
				31 Hrs			

I Year II Semester

S.No	Course Code	Course Type	Course Title	L	T	P	C
1.	22VLB104	Professional Core - 4	Physical Design Automation	3	-	2	4
2.	22VLB105	Professional Core -5	VLSI Testing And Validation	3	-	2	4
3.		Department Elective -3	-	2	-	2	3
4.		Department Elective -4	-	2	-	2	3
5.	22MSB101	RM & IPR	Research Methodology and IPR	-	2	2	2
6.	22VLB106	Interdepartmental Project	Interdepartmental Project	-	1	3	2
7.	22VLB107	Teaching Activity	Teaching Assistanceship	-	-	4	2
Total				20			
9.		Add-on certification course -1		3	-	2	4
Grand Total				13	3	19	**24**
				35 Hrs			

II Year I Semester

S.No	Course Code	Course Title	L	T	P	C
1	22VLB202 / 22VLB201	Project / Internship in Industry	-	2	24	13
2		Add-on certification course-2 (MOOCs/Self-study course)	4			4
Total			4	2	24	17

II Year II Semester

S.No	Course Code	Course Title	L	T	P	C
1	22VLB204 / 22VLB203	Project / Internship in Industry	-	2	24	13
2		Add-on certification course-3 (MOOCs/Self-study course)	4			4
Total			4	2	24	17

Department Elective Courses

S.No	Course Code	Course Title	L	T	P	C
1.	22VLB801	FPGA based System Design	2	-	2	3
2.	22VLB802	Microchip Fabrication Technology	2	2	0	3
3.	22VLB803	Advanced Digital System Design	2	-	2	3
4.	22VLB804	Scripting Languages	2	-	2	3
5.	22VLB805	Verification using System Verilog and UVM	2		2	3
6.	22VLB806	SOC Design	2	2	0	3
7.	22VLB807	VLSI Circuits for IoT	2	-	2	3
8.	22VLB808	Mixed Signal Design	2	-	2	3
9.	22VLB809	CMOS RF Integrated Circuits	2	-	2	3
10.	22VLB810	MEMS/NEMS	2	-	2	3
11.	22VLB811	ASIC Design	2	-	2	3
12.	22VLB812	Sensors and Sensor Circuit Design	2	-	2	3
13	22VLB813	VLSI Signal Processing	2	-	2	3

ADD-ON DEGREE COURSES						
S.No	**Course Code**	**Course Title**	**L**	**T**	**P**	**C**
1	22VLB951	Nano Electronics Devices and device modelling	3	-	2	4
2	22VLB952	Hardware Security	3	-	2	4
3	22VLB953	Low Power VLSI Design	3	-	2	4
4	22VLB954	Software/Hardware Co-design	3	-	2	4

22VLB101 – SEMICONDUCTOR DEVICE MODELING

Hours per Week:

L	T	P	C
2	0	2	**3**

PREREQUISITE COURSE: Semiconductor Physics.

COURSE DESCRIPTION AND OBJECTIVES:

This course focuses on the derivation of models for the terminal currents of the semiconductor devices used in integrated circuits, specifically, the MOSFET and bipolar junction transistor..

MODULE-1

UNIT-1: Semiconductor Physics

[8L+0T+8P=16 Hours]

Energy Bands and Carrier Concentration in thermal Equilibrium. Fermi distribution, density of states, Boltzmann statistics. Intrinsic Carrier Concentration, Donors and Acceptors. Carrier Transport Phenomena: Carrier Drift, Carrier Diffusion, drift-diffusion equations. Generation and Recombination Processes, Continuity Equation, Thermionic Emission Process, Tunnelling Process, High-Field Effects

UNIT-2: P-N Junction [8L+0T+8P=16 Hours]

Device physics: Thermal equilibrium, Internal electro-static fields and potentials, Poisson's equation, continuity equations, drift-diffusion equations. I-V Characteristics: Forward bias, reverse bias, Diode equation. Capacitive effect: Junction and diffusion capacitance. DC, AC and transient analysis of Diodes.

Practices:

- Design a P-N junction diode with smallest dimensions by referring a latest journal paper and analyze its performance through band diagram and electrical characteristics.
- Solve drift-diffusion equation for transport parameters (Drift velocity, mobility and conductivity) of direct and indirect band gap materials.

MODULE-2

UNIT-1: BJT and Metal-Semiconductor Contacts and Schottky Diodes [8L+0T+8P=16 Hours]

Device Physics: Ideal MS contacts, Schottky diode-Electrostatics, I-V characteristics, DC, AC and transient analysis. Metal-Semiconductor contacts: Ohmic contacts, Schottky contacts, Tunnel contacts, annealed and alloyed contacts. BJT: Ebers-Moll model; large control model; small signal models for low and high frequency and switching characteristics.

UNIT-2: MOSFET [8L+0T+8P=16 Hours]

MOS capacitor, MOSFET Physics: I-V characteristics, Sub-threshold region, Body effect, Capacitive effect, small and large signal model. MOSFET Short Channel effects: Punch through, DIBL, Hot electron effect, Velocity Saturation, Leakage current.

Practices:

- Design a MOSFET with smallest dimensions by referring a latest journal paper and analyze its performance through band diagram and electrical characteristics by make use of process and device simulators.

SKILLS:

- Understand the physics of semiconductor materials and devices.
- Solve bandgap models and design different semiconductor devices.
- Use the appropriate jargon to convey a particular type of device model

ACTIVITIES:

- Describe the essential properties of semiconductor materials which enable us to make different devices.
- Recognize the various stages of IC design where device models are used.
- Distinguish among activities of analysis, modeling, simulation and design.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Apply the concepts and techniques to solve bandgap model equations and design various semiconductor devices	Apply	1	1, 2, 3,4, 5, 9, 10, 12
2	Apply suitable approximations and techniques to derive the model referred to above starting from drift-diffusion transport equations (assuming these equations hold)	Apply	1, 2	1, 2, 3,4, 5, 9, 10, 12
3	Simulate characteristics of a simple device using MATLAB, SPICE and ATLAS /SYNOPSYS	Analyze Apply	1,2	1, 2, 3,4, 5, 9, 10, 12

TEXT BOOKS:

1. S. M. Sze and Ming-Kwei Lee, Semiconductor Devices Physics and technology, John Wiley & Sons, 2013.

REFERENCE BOOKS:

1. Ben G. Streetman and Sanjay Banerjee, Solid State Electronic Devices, Pearson Ed, 2014.
2. M. S. Tyagi, Introduction to semiconductor materials and devices, John Wiley & Sons, 2008.
3. Campbell, Stephan, Fabrication Engineering at the Micro and Nanoscale, Oxford University Press, 2008.
4. Robert F. Pierret, Semiconductor Device Fundamentals, Pearson Education, 2006.

22VLB102 – ANALOG IC DESIGN

Hours per Week:

L	T	P	C
3	0	2	4

PREREQUISITE COURSE: Analog Circuits, VLSI Design.

COURSE DESCRIPTION AND OBJECTIVES:

This course covers the analysis and design of analog integrated circuits starting from basic building blocks to different implementations of the amplifiers in CMOS technology.

MODULE-1

UNIT-1 **12L+8T+0P=20 Hours**

CMOS Device Fundamentals: Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output resistance, frequency dependence of device parameters.

Current Mirrors: CMOS current mirror, Source degenerated current mirror, High output impedance current mirrors.

UNIT-2 **12L+8T+0P=20 Hours**

Single stage amplifiers: Common source amplifier, common drain amplifier or source follower, Common gate amplifier, Cascode gain stage, MOS differential pair, Differential Amplifiers.

Practices:

Design and simulate the following analog circuits.

- Verify the characteristics of nMOS and pMOS devices.
- Current Mirror and Cascode Current Mirror circuits
- Common Source, Common Drain and Common Gate Amplifiers
- Differential Amplifier

MODULE-2

UNIT-1 **12L+8T+0P=20 Hours**

Frequency Response of Amplifiers: Miller effect, Common Source amplifier, Source follower amplifier, Common gate amplifier, Cascode gain stage.

UNIT-2 **12L+8T+0P=20 Hours**

CMOS Operational Amplifiers: Classification of Op Amps, Design of one stage and two stage Opamps, Gain boosting techniques, Folded cascode amplifier, Telescopic cascode amplifier and Common mode feedback (CMFB) amplifier, Opamp specification analysis, stability, and frequency compensation.

Practices:

Design and simulate the following analog circuits.

- CMOS Op-amp single Stage
- Two stage operational amplifier
- Folded cascode amplifier

- Telescopic cascode amplifier

SKILLS:

- Identify and analyze various Current mirror circuits.
- Design of differential amplifier.
- Analyze the frequency response of amplifers.

ACTIVITIES:

- Amplifier design.
- Opamp analysis.
- Current mirror implementation.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mappingwith POs
1	Design basic building blocks of analog ICs.	Apply	1	1, 2, 4, 5, 9, 10, 12
2	Design optimal single stage amplifiers for various applications	Apply	1	1, 2, 5, 9, 10
3	Analyze the frequency response of amplifiers	Analyze	2	1, 2, 3, 5, 9, 10
4	Develop a procedure for optimal compensation of op-amp against process, supply and temperature variations	Apply	2	1, 2, 5, 9, 10, 12

TEXT BOOKS:

1. BehzadRazavi, “Design of Analog CMOS integrated circuits”, McGraw-Hill International edition, 2001.
2. D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley,1997.

REFERENCES BOOKS:

1. R Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley,1986.
2. R L Geiger, P E Allen and N R Strader, VLSI Design Techniques for Analog &Digital Circuits, McGraw Hill,1990.
3. Gray, Wooley, Brodersen, “Analog MOS Integrated circuits”, IEEE press,1989.
4. Alan B. Grebene, “Bipolar and MOS Analog Integrated Circuit Design”, Wiley, 2002.

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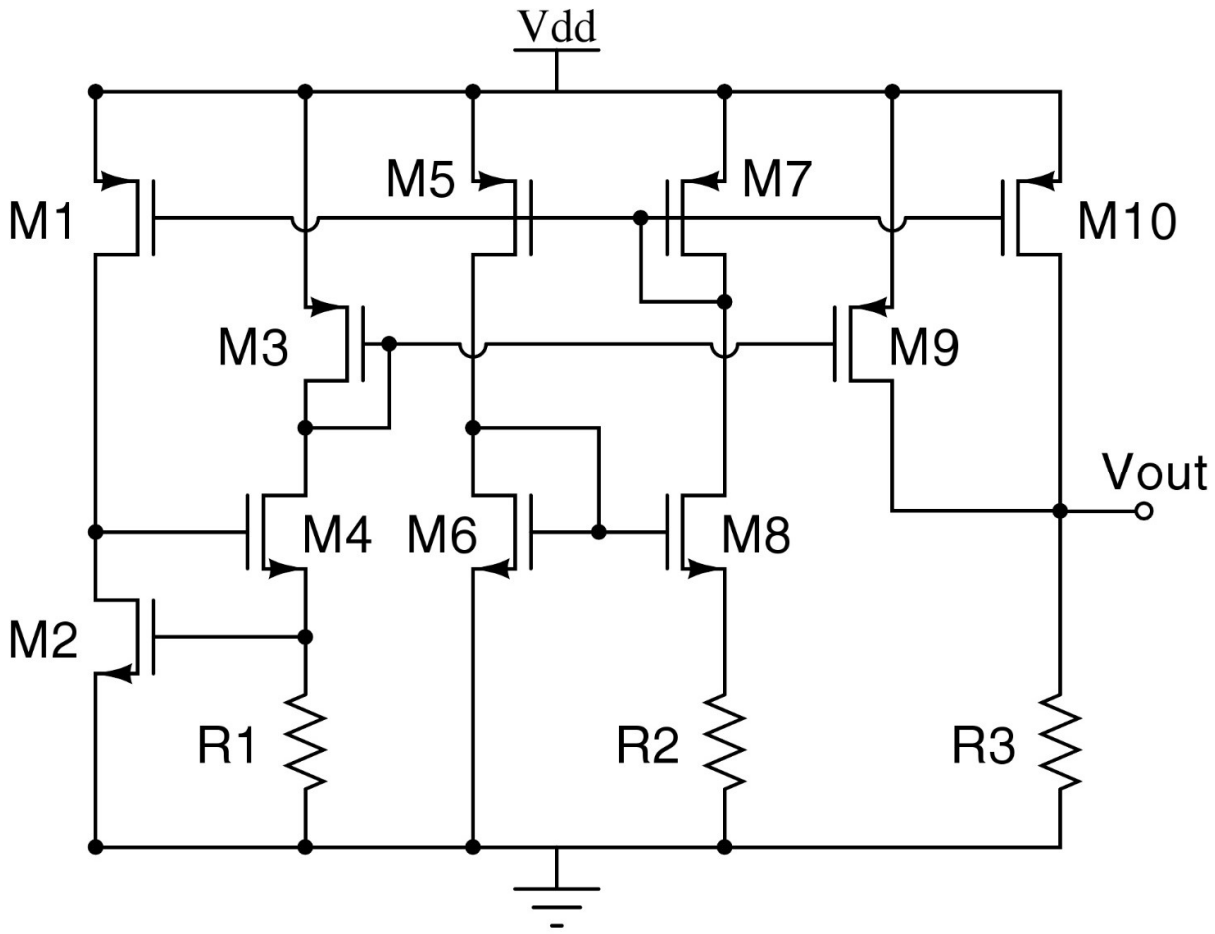

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22VLB103 – Digital IC Design

Hours per Week:

L	T	P	C
3	-	2	**4**

PREREQUISITE KNOWLEDGE: Digital Electronics, VLSI Design

COURSE DESCRIPTION AND OBJECTIVES:
This course covers the analysis and design of digital integrated circuits starting from basic building blocks to different implementations of the amplifiers in CMOS technology.

MODULE-1

UNIT-1: [8L+8T+0P=16 Hours]

CMOS Inverter: Introduction to MOS transistor, V-I Characteristics, Electrical Parameters, Static behaviour, switching Threshold, Noise Margins, Robustness revisited, Dynamic behaviours: Computing the capacitances, propagation delay, propagation delay from a design perspective, power, energy and energy delay product.

UNIT-2: [8L+8T+0P=16 Hours]

Combinational Logic Design: Introduction, Static CMOS Design: Complementary CMOS, ratioed
logic, pass transistor logic dynamic CMOS Design: Dynamic logic, speed and power dissipation of
dynamic logic, signal integrity issues in Dynamic design, cascading dynamic gates.

MODULE-2

UNIT-1: [8L+8T+0P=16 Hours]
Sequential Logic Design: Introduction, static latches and registers: The Bi-stability principle, multiplexer based latches, master-slave Edge-Triggered register, Static SR Flip-flop, dynamic latches and registers, dynamic transmission, Gate Edge - triggered registers, -CMOS True single - phase clocked register (TSPCER), clock skew and jitter.

UNIT-2: [8L+8T+0P=16 Hours]

Digital Integrated System Building Blocks: Introduction, Adders, Multipliers, Shifters, Memories, ROM, RAM, Internal structure, ROM 2 D Structure, SRAM, DRAM.

Practices:

1. Design of Inverter and all logic gates.
2. Design and Simulation of Full adder.
3. Design and Simulation of Serial Binary Adder, Carry Look Ahead Adder.
4. Design of SRAM and DRAM.
5. Design of pseudo logic gates.
6. Design of DCVSL logic gates
7. Design of flip flops: SR, D, JK, T.
8. Design of edge triggered registers.
9. Design of barrel shifter.
10. Design of Multiplier.

Note: Implementing the above designs on Circuit level.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Design CMOS inverters with specified noise margin and propagation delay	Apply	1	1, 2, 4, 5, 9, 10, 12
2	Design efficient techniques at combinational circuit level for improving power and speed of digital circuits	Apply	1	1, 2, 5, 9, 10
3	Design efficient sequential circuits for improving performance of digital circuits	Apply	2	1, 2, 3, 5, 9, 10
4	Design arithmetic blocks and memories to improve speed and power parameters.	Apply	2	1, 2, 5, 9, 10, 12

TEXT BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic., Digital Integrated Circuits: A Design Perspective, Second Edition, Pearson Education India, 2003

2. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 1st edition, 1999.

REFERENCE BOOKS:

1. Neil H. E. Weste and D. M. Harris, CMOS VLSI Design, Third Edition, 2010.

2. Sung-Mo Kang, CMOS Digital Integrated Circuits, 3rd Edition, McGraw-Hill, 2003.

3. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

22VLB104 - PHYSICAL DESIGN AUTOMATION

Hours per Week:

L	T	P	C
2	-	2	3

PREREQUISITE KNOWLEDGE:

- Logic circuits
- Linear circuit analysis
- Digital system design
- VLSI
- Basic programming skills (C/C++)

Course Description

- Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
- Discuss the concepts of design optimization algorithms and their application to physical design automation.
- Understand the concepts of simulation and synthesis in VLSI Design Automation
- Formulate CAD design problems using algorithmic methods

MODULE-1

UNIT-I: Physical Layout Design [6L+0T+6P=12 Hrs]

Introduction: Introduction to physical layout design of digital VLSI circuits and systems, Design methodologies and optimization problems, Algorithms and optimization techniques, Floor planning: - Basic concepts, Sequence pair, Analytical floor planning, Polish expression.

UNIT-2: [10L+0T+10P=20 Hrs]

Layout Designing: Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms.

Floor Planning and Routing: floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms**.**

MODULE-2

UNIT-I: Floor Planning [6L+0T+6P=12 Hrs]

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

UNIT-2: Simulation and Logic synthesis [10L+0T+10P=20 Hrs]

Simulation and logic synthesis- gate level and switch level modelling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

COURSE OUTCOMES:

At the end of the course, the students should be able to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Students are able to know how to place the blocks and how to partition the blocks while for designing the layout for IC.	Apply	1,2	1, 2, 3, 4, 9, 10, 11, 12
2	Students are able to solve the performance issues in circuit layout.	Create	1,2	1, 2, 3, 4, 9, 10, 11, 12
3	Students are able to analyze physical design problems and Employ appropriate automation algorithms for partitioning, floor planning, placement and routing	Create	1,2	1, 2, 3, 4, 9, 10, 11, 12
4	Students are able to decompose large mapping problem into pieces, including logic optimization with partitioning, placement and routing	Create	1,2	1, 2, 3, 4, 9, 10, 11, 12
5.	Students are able to analyze circuits using both analytical and CAD tools	Create	1,2	1, 2, 3, 4, 9, 10, 11, 12

BOOKS AND REFERENCES

Text Book:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley ,1998.
2. N.A.Sherwani , "Algorithms for VLSI Physical Design Automation", (3/e), Kluwer,1999.
3. VLSI Physical Design Automation: Theory and Practice, Sadiq M. Sait, Wspc, 1999, ISBN 978-9810238834.
4. Algorithms for VLSI Physical Design Automation, 3/E, Naveed A. Sherwani, Springer, 1998, ISBN 978-0792383932
5. Practical Problems in VLSI Physical Design Automation, Sung Kyu Lim, Springer, 2008, ISBN 978-1402066269

References:

1. S.M. Sait , H. Youssef, "VLSI Physical Design Automation", World scientific, 1999.
2. M. Sarrafzadeh, "Introduction to VLSI Physical Design", McGraw Hill (IE), 1996.

22VLB105 – VLSI TESTING AND VALIDATION

Hours per Week:

L	T	P	C
2	0	2	**3**

PREREQUISITE COURSE: Digital Logic Design and VLSI Design.

COURSE DESCRIPTION AND OBJECTIVES:
The goal of this syllabus, as its name implies, is to allow the reader to become proficient in the testing and validation of modern ICs.

MODULE-1

UNIT-1: Introduction to VLSI Testing, Fault Modelling and Simulation

[8L+0T+8P=16 Hours]

Role of testing, Verification Vs Testing, Levels of testing, Overheads of testing, Basic testing principle. Levels of Fault Models, Various types of faults, Fault Coverage. Fault Collapsing, Fault Dominance. Simulation for design verification, Simulation for Test evaluation. Modern Fault Simulation for Combinational Circuits

UNIT-2: TEST GENERATION [8L+0T+8P=16 Hours]

Controllability and Observability, Measures for controllability and observability of combinational and sequential circuits, Test Generation for Combinational Circuits, ATPG algorithms for combinational circuits (Roth's D algorithm), and Some applications. Test Generation for Sequential Circuits: Classical approach, Time Frame Expansion Method.

Practices:

- Development of an exhaustive test bench for the 1-bit full adder.
- Development of exhaustive test bench for 16X1 Multiplexer using file reading writing features.
- Development of layered testbench components for functional verification of synchronous FIFO.

MODULE-2

UNIT-1: SYSTEM LEVEL TEST [8L+0T+8P=16 Hours]

Design for Testability, Adhoc Testing, Scan Based Test Techniques, Memory Testing, IDDQ Testing, IDDQ testing Methods-Boundary Scan, Boundary Scan Architecture.

UNIT-2: BUILT INSELFTEST [8L+0T+8P=16 Hours]

Built-In Self-Test (BIST), BIST Techniques,BIST Response Compaction, Circular BIST, Overview of Memory BIST.

Practices:

- Design for Test and Automatic Test pattern Generation for a 4-bit counter.
- Perform the logic equivalence (formal verification)

SKILLS:

- Test pattern generation of any combinational and sequential circuits.
- Development of layered testbench components for functional verification of any combinational and sequential circuits.
- VLSI system level testing.
- Design and investigate self-checking circuits.

ACTIVITIES:

- Test bench generation.
- System level testing.
- Fault modelling.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Illustrate the logical and fault simulation techniques	Analyse	1	1, 2, 3,4, 5, 9, 10, 12
2	Test VLSI systems using existing test methodologies, equipment's and tools**.**	Apply	1, 2	1, 2, 3,4, 5, 9, 10, 12
3	Construct a Design for Testability (DFT) algorithm for VLSI Circuits.	Apply	2	1, 2, 3,4, 5, 9, 10, 12

TEXT BOOKS:

1. M.L.Bushnell and V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publishers, 2nd edition, 2004.
   .

REFERENCE BOOKS:

1. W.W.Wen, "VLSI Test Principles and Architectures Design for Testability", Morgan Kaufmann,1st edition, 2006.
2. A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International 2002.
3. ZainalabeNavabi, "Digital System Test and Testable Design:Using HDL Models and Architectures", Springer, 2010.
4. A. K Sharma, Semiconductor Memories Technology, Testing and Reliability, IEEE, 1997.
5. M.Abramovici,M.A.Breuer and A.D.Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 1st edition, 1990.

22VLB801 – FPGA BASED SYSTEM DESIGN

Hours per Week:

L	T	P	C
2	-	2	**3**

PREREQUISITE KNOWLEDGE: Microprocessors and Microcontrollers.

COURSE DESCRIPTION:

This course covers the design and analysis of digital circuits with Verilog HDL. The primary goal is to provide basic understanding of system design. The course enables students to apply their knowledge for the design of digital hardware systems with help of FPGA tools.

1. Understand Digital system design using Verilog HDL.

2. Know FPGA architecture, interconnect and technologies.

3. Understand and implement embedded system on FPGA.

MODULE-1

UNIT-1: Introduction to FPGA Architectures and Verilog [6L+0T+6P=12 Hrs]

Introducing FPGAs: Exploring the Xilinx Artix-7 and 7 series devices, Combinational logic blocks, Storage, Clocking, I/Os, DSP48E1, ASMBL architecture.

Gate-level Combinational circuit

Introduction, general description, basic lexical elements, data types, four-value system, data type groups, number representation, operators, program skeleton, port declaration, program body, signal declaration, structural description, testbench.

UNIT-2: RTL combinational circuit and Systems [10L+0T+10P=20 Hrs]

Introduction, operators, always block for a combinational circuit, If statement, case statement, coding guidelines for an always block, parameter, constant, BCD incrementor.

PRACTICES:

- Introduction to Vivado
- Setup and test the available FPGA board using the appropriate software tool.
- Design and test up and down counters
- Design and test a Binary Coded Decimal Adder.
- Design a Sequence Detector using Mealy Machine
- Design a Sequence Detector using Moore Machine

MODULE-2

UNIT-1: Regular sequential circuit [6L+0T+6P=12 Hrs]

Introduction, HDL code of the FF and register, simple design examples, test bench for sequential circuits, square wave generator, PWM and LED dimmer.

UNIT-2: FSM [10L+0T+10P=20 Hrs]

Introduction- Mealy and Moore outputs, FSM Representation, FSM code development, Design examples - Rising-edge detector, Debouncing circuit, Vending Machine, Elevator

UART:

UART receiving subsystem, UART transmitting subsystem, Overall UART system, Customizing a UART

PRACTICES:

1. Generate a square wave signal with FPGA.
2. Generate a sinusoidal signal with FPGA.
3. Send a series of characters to PC through UART
4. Interface a stepper motor FPGA
5. Design and test a PWM Circuit, with verification by simulation.
6. Implementing CAN protocol using FPGA
7. Data communication through I2C protocol on FPGA

SKILLS:

1. Verilog program development
2. Circuit design
3. Timing analysis

COURSE OUTCOMES:

At the end of the course, the students should be able to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Design and optimize complex combinational and sequential digital circuits.	Apply	1,2	1, 2, 3, 4, 9, 10, 11, 12
2	Model and implement Combinational and sequential digital circuits by Verilog HDL.	Create	1,2	1, 2, 3, 4, 9, 10, 11, 12
3	Design and model digital circuits with Verilog HDL at behavioural, structural, and RTL Levels.	Create	1,2	1, 2, 3, 4, 9, 10, 11, 12
4	Develop test benches to simulate combinational and sequential circuits.	Create	1,2	1, 2, 3, 4, 9, 10, 11, 12

BOOKS AND REFERENCES:

TEXT BOOKS:

1. FPGA Programming for beginners by Fank Bruno, Packt Publishing Limited, 2021, ISBN 978-1-78980-541-3.
2. FPGA Prototyping By Verilog Examples, by Pong P. Chu, A JOHN WILEY & SONS, INC., PUBLICATION, 2008
3. Design Through Verilog HDL, T.R. Padmanabhan, B. Bala Tripura Sundari, Wiley Interscience, 2004

REFERENCE BOOKS:

1. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, Prentice Hall, Second Edition, 2003.
2. A Verilog HDL primer by J. Bhaskar, Star Galaxy Pub., 2004
3. Verilog HDL Design Examples by Joseph Cavanagh, CRC Press, 2017
4. VHDL and FPLDs, by Zoran Salcic, Kluwer,1998
5. Computers as Components, Principles of Embedded Computing System Design, by Wayne Wolf, Morgan Kauffman, 2001
6. A VHDL Primer, by Jayaram Bhasker. Prentice Hall, 1998
7. HDL Chip Design, by Douglas J. Smith, 1999

8. VHDL Analysis and Modeling of Digital Systems, by Z. Navabi, McGraw-Hill, 1993

WEB REFERENCES:

1. http://www.ece.rutgers.edu/node/1528
2. http://www.ece.iastate.edu/~morris/388/syllabus_388x.html

22VLB802 – MICROCHIP FABRICATION TECHNOLOGY

Hours per Week:

L	T	P	C
2	2	0	**3**

PREREQUISITE COURSE: VLSI Design.

COURSE DESCRIPTION AND OBJECTIVES:

The course is intended to provide an understanding of current fabrication practices used in the semiconductor industry, along with the challenges and opportunities in device fabrication

MODULE-1

UNIT-1: Environment for VLSI Technology [8L+8T+0P=16 Hours]

Brief History of Semiconductor technology, Scaling Trends and Scaling Methodologies, Scaling Challenges, ITRS Roadmap; Starting material, silicon structure and properties. Clean room and safety requirements. Wafer cleaning processes. Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling and technology, damage annealing.

UNIT-2: Oxidation and Lithography [8L+8T+0P=16Hours]

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin, and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterizations of oxide films; High k and low k dielectrics for ULSI. Lithography: Photolithography, E-beam lithography, and newer lithography techniques for VLSI/ULSI; Mask generation.

MODULE-2

UNIT-1: Deposition requirements and techniques [8L+8T+0P=16Hours]

Physical vapor deposition (PVD) techniques: Evaporation- Thermal evaporation, Electron beam evaporation, Sputtering- Glow discharge sputtering, Magnetron sputtering, Ion beam sputtering, Chemical vapor deposition techniques: Photoassisted CVD, Thermally activated CVD, Plasma enhanced (RF, μ-Wave) CVD, Low pressure (LP) CVD, Atmospheric pressure (AP) CVD. Epitaxial growth techniques; Wet and dry etching techniques, Etch requirements.

UNIT-2: Characterization Techniques and Interconnect Technology [8L+8T+0P=16 Hours]

Scanning electron microscope (SEM), Atomic Force Microscopy (AFM), XPS, AES, EPMA. Copper and Aluminum interconnects, Silicodes, Isolation, CMOS and BJT Process flow; CMOS process for sub-100nm era - dielectrics and gate electrodes, Low K Dielectrics with Cu, Strained silicon, Silicon Germanium, Process Techniques to overcome Short Channel Effects, Nanolithography techniques, SOI Technology, Ultra Shallow Junction. Multiple Gate MOSFETs.

SKILLS:

- Know various deposition techniques at the atomic and molecular level.
- Acquire knowledge about structure and properties of thin films.
- Learn the advanced concepts in various vapour deposition techniques.
- Be aware of various morphological techniques and selecting appropriate tools for their future research.

ACTIVITIES:

- Nanostructure characterization.
- State-of-the-art metrology tools.
- Study the material's structure and properties.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Apply and analyze the fabrication processes such as Etching, Deposition, and Epitaxy	Apply	1,2	1, 2, 3,4, 5, 9, 10, 12
2	Prepare, characterise and analyse the samples with suitable techniques	Apply	1, 2	1, 2, 3,4, 5, 9, 10, 12
3	Comprehend and apply concepts related to interconnects and metallization, process flow, and integration with CMOS Technology	Apply	2	1, 2, 3,4, 5, 9, 10, 12

TEXT BOOKS:

1. Peter Van Zant, "Microchip Fabrication: A Practical Guide to Semiconductor Processing", McGraw-Hill Professional, Sixth Edition, 2014.

REFERENCE BOOKS:

1. Gary. S. May and S. M. Sze, "Fundamentals of semiconductor fabrication", John Wiley, First Edition, 2003.
2. Marc J. Madou, "Fundamentals of Microfabrication and Nanotechnology - Volume II", CRC Press, Third Edition, 2011.
3. Stephen Campbell, "Science of Microelectronic Fabrication", Oxford University Press, 2001.

James D. Plummer, Michael D. Deal, Peter B. Griffin, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Prentice Hall India Private Limited, 2000

22VLB803 - ADVANCED DIGITAL SYSTEM DESIGN

Hours per Week:

L	T	P	C
3	2	-	**4**

PREREQUISITE KNOWLEDGE: Digital Electronics.

COURSE DESCRIPTION AND OBJECTIVES:
To analyze synchronous and asynchronous sequential circuits. To realize and design hazard free circuits. To familiarize the practical issues of sequential circuit design. To gain knowledge about different fault diagnosis and testing methods. To estimate the performance of digital systems. To know about timing analysis of memory and PLD.

MODULE-1

UNIT-1: SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN & ASMCHARTS [12L+8T+0P=20 Hours]

Reduction of State Tables, State Assignments, Sequential Circuit Design: - Design of Code Converter, Design of Iterative Circuits. Design of Sequential Circuits Using ROMs and PLAs, Sequential Circuit Design using CPLDs and FPGAs, ASM Charts.

UNIT-2: ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN [12L+8T+0P=20 Hours]

Analysis of Asynchronous Sequential Circuit (ASC) – Fundamental Mode Model, Flow Table, State Reduction, Design of ASC. Hazards, Races and Cycles.

Practices

- Design of code converters.
- Design of different Sequential circuits.
- Design of different Asynchronous Sequential circuits.

MODULE-2

UNIT-1: STATE-IDENTIFICATION EXPERIMENTS AND TESTING OF SEQUENTIAL CIRCUITS [12L+8T+0P=20 Hours]

Experiments, Homing Experiments, Distinguishing Experiments, Machine Identification, Checking Experiments, Design of Diagnosable Machines, Alternative Approaches to the Testing of Sequential Circuits, Built-In Self-Test (BIST).

UNIT-2: ARCHITECTURES FOR DIGITAL PROCESSORS AND ARITHMETIC PROFESSORS [12L+8T+0P=20 Hours]

Digital Filters and Signal Processors – Finite-Duration Impulse Response Filter, Digital Filter design process, Infinite-Duration Impulse Response Filter, Building blocks for signal Processors, Pipelined Architectures. Arithmetic Processors – Functional units for Addition, Subtraction, Multiplication and Division, Multiplication of Signed Binary Numbers and Fractions.

PRACTICES:

- Product of Signed numbers.
- Booth's Algorithm sequential multiplier.
- Division of Unsigned Binary numbers.
- Design of Reduced-Register Sequential divider.

SKILLS:

- Learn about various digital systems and technologies, such as FPGAs.
- Apply knowledge to test digital circuits and identify different sorts of errors and how to correct them.

ACTIVITIES:

- Create an ALU using PLA.
- A fault-finding algorithm for sequential circuits.
- Students can use testing procedures to create testing circuits (BIST).

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	To Identify, design and analyze Synchronous and sequential logic circuits and design and develop system controller.	Apply	1	1, 2, 12
2	To Identify, design and analyze Asynchronous sequential logic circuits and design and develop system controller.	Apply	1	1, 2, 4, 5, 12
3	To Evaluate the digital system design by state identification techniques	Apply	2	1, 2, 3, 5, 12
4	To develop various architectures for Digital and Arithmetic processors.	Create	2	1, 2, 3, 12

TEXT BOOKS:

1. Charles H. Roth Jr. and Larry L. Kinney, "Fundamentals of Logic design", 6th edition, Thomson Learning, 2004.
2. Parag K Lala, "Digital Circuit Testing and Testability", Academic Press,2002.
3. ZviKohavi and Niraj K.Jha, "Switching and Finite Automata Theory", 3rd edition, Cambridge University Press, 2010.
4. Michael D Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd edition, Pearson, 2011.

REFERENCE BOOKS:

1. Donald G. Givone, "Digital principles and Design", TataMcGraw Hill, 1st edition, 2003.
2. Stephen Brown and ZvonkVranesic, "Fundamentals of Digital Logic with VHDLDeisgn", Tata McGraw Hill,2002.
3. Mark Zwolinski, "Digital System Design with VHDL", Pearson Education,2004.

22VLB804 – SCRIPTING LANGUAGES

Hours per Week:

L	T	P	C
3	2	-	**4**

PREREQUISITE KNOWLEDGE: Programming Language.

COURSE DESCRIPTION AND OBJECTIVES:

To explain the characteristics and uses of scripting languages. To describe the various PERL concepts used in VLSI design. To learn the concepts of TC.

MODULE-1

UNIT-1 **[12L+8T+0P=20 Hours]**

INTRODUCTION TO SCRIPTS AND SCRIPTING USING PERL:
Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT-2 **[12L+8T+0P=20 Hours]**

ADVANCED PERL: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure, Architecture Specialization techniques, System Communication infrastructure.

PRACTICES:

- Get started quickly with programming
- Set up a Perl development environment for practicing Perl
- Understanding of variables, variable scopes, and variable interpolation.
- Create plug-ins and extensions.

MODULE-2

UNIT-1 **[12L+8T+0P=20Hours]**

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT-2 **[12L+8T+0P=20 Hours]**

ADVANCED TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

PRACTICES:

- Running TCL.
- Simple Text Output.
- Evaluation & Substitutions 1: Grouping arguments with “”
- Textual Comparison – switch
- Evaluation & Substitutions 2: Grouping arguments with {}
- Evaluation & Substitutions 3: Grouping arguments with []
- Results of a command - Math 101

SKILLS:

- Apply the knowledge of PERL to write any program.
- Apply the knowledge of TCL to write any program.
- Resolve security issues in internet programming.

ACTIVITIES:

- Creating new applications in web browsers
- Assigning values to variables.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Interpret typical scripting languages for system ap-plications.	Apply	1	1, 2, 12
2	Develop server-side scripts using Perl and TCL.	Apply	1	1, 2, 5, 12
3	Create software systems using scripting languages, Including Perl and TCL.	Create	2	1, 2, 3, 5, 12
4	Design websites using advanced TCL.	Create	2	1, 2, 12

Text Books:

1. David Barron, "The World of Scripting Languages", Wiley Student Edition, 2010.
2. Brent Welch, Ken Jones and Jeff Hobbs, "Practical Programming in TCL and TK", Fourth edition, 2003.

Reference Books:

1. Clif Flynt, "TCL/TK: A Developer's Guide", Morgan Kaufmann Series, 2003.
2. John Ousterhout, "TCL and the TK Toolkit", 2nd Edition, Kindel Edition, 2009.
3. Wojciech Kocjan and Piotr Beltowski, "TCL 8.5 Network Programming book", Packt Publishing.

22VLB805 – VERIFICATION USING SYSTEM VERILOG AND UVM

Hours per Week:

L	T	P	C
3	-	2	**4**

PREREQUISITE KNOWLEDGE: Digital Electronics.

COURSE DESCRIPTION AND OBJECTIVES:

To expose the students to all aspects of functional verification of digital systems. To provide a practical approach for verification of designs. To understand and use basic System Verilog features, including new data types, literals, statements, and operators; enhancements to tasks and functions; and packages and interfaces. To understand the features and capabilities of the UVM class library for System Verilog. To create and configure reusable, scalable, and robust UVM Verification Components (UVCs).

MODULE-1

UNIT-1 **[12L+8T+0P=20 Hours]**

SYSTEM VERILOG AND TEST BENCH:

Data Types, Arrays, Structures, Unions, Procedural Blocks, Tasks & Functions, Procedural Statements,
Interfaces, Basic OOPs, Randomization, Threads & Inter Process Communication, Test bench guidelines, Advanced Interfaces, A Complete System Verilog Test Bench (SVTB).

UNIT-2 **[12L+8T+0P=20 Hours]**

SYSTEM VERILOG ASSERTIONS:

Introduction to SVA, building blocks, Properties, Boolean expressions, Sequence, Single & Multiple
Clock definitions, Implication operators, Repetition operators, Built-in System functions, Constructs, Assertion directives.

PRACTICES:

- Examples implementing implication operators
- Functional verification.
- Create Built in system functions.

MODULE-2

UNIT-1 **[12L+8T+0P=20 Hours]**

CORE UVM VERIFICATION ENVIRONMENT AND UVM LIBRARY: Introduction to UVM Methodology: UVM Testbench and Environments, System and Module UVCs; Object-Oriented Programming: Classes, Objects and Program, Unified Modeling Language Diagrams; UVM Library: UVM_object class, UVM_Component class, Transaction Level Modeling.

UNIT-2 **[12L+8T+0P=20 Hours]**

INTERFACE UVCs AND TESTBENCH INTEGRATION: Interface UVCs: Stimulus Modeling and Generation, Modeling Topology with UVM, Creating the Agent, UVM Verification Component and UVM Sequence; Testbench Integration: Testbench Configuration, Virtual Sequencers and Sequences, Implementing a Coverage Model.

PRACTICES:

- Creating simple data stimulus
- Universal Verification Component (UVC) architecture
- Factories and configuration control

SKILLS:

- Develop a synthesizable Verilog code and test bench for verification of complex combinational and sequential circuits.
- Integrating multiple UVCs
- Writing multichannel and system-level tests

ACTIVITIES:

- Creating new case building a scoreboard
- Functional coverage

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Outline the System Verilog environment of digital systems.	Apply	1	1, 2, 4, 5, 9, 10, 12
2	Model a scenario for Verification of a DUT in System Verilog.	Apply	1	1, 2, 4, 5, 9, 10, 12
3	Develop UVM environment at chip level.	Apply	2	1, 2, 3, 5, 9, 10
4	Create test benches for digital systems.	Create	2	1, 2, 4, 5, 9, 10, 12

TEXT BOOKS:

1. Chris Spear, Greg Tumbush, "System Verilog for Verification - A Guide to Learning the Testbench Language Features", Springer, Third Edition, 2012.
2. Sharon Rosenberg, Kathleen A Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Cadence Design System, 2010.

REFERENCE BOOKS:

1. Ben Cohen, cohen, Venkataramanan, Kumari, Srinivasan Venkataramanan, Ajeetha Kumari, "System Verilog Assertions Handbook - for Formal and Dynamic Verification", Vhdl cohen publishing, 2005.
2. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for design: a guide to using System Verilog for hardware design and modeling", Springer, ISBN 1402075308, 9781402075308, 2004.
4. Ray Salemi, "The UVM Primer – An Introduction to the Universal Verification Methodology", 2013.

22VLB806 – SOC Design

Hours per Week:

L	T	P	C
2	2	-	**3**

PREREQUISITE KNOWLEDGE: Concepts of VLSI Design

COURSE DESCRIPTION AND OBJECTIVES:

This course off ers the concepts of integrating all components of any electronic system into a single chip. The objective of the course is to introduce the students to digital, analogue, mixed- signal, and radio-frequency functions to integrate all on a single chip substrate.

MODULE-1

UNIT-1: **[8L+8T+0P=16 Hours]**

INTRODUCTION TO SOC: System trade-off s and evolution of ASIC technology, System on chip concepts and methodology, SoC design issues, SoC challenges and components.

UNIT-2: **[8L+8T+0P=16 Hours]**

DESIGN METHODOLOGY FOR LOGIC CORES: SoC design fl ow, On-chip buses, Design process for hard cores, Soft and fi rm cores, Designing with hard cores, soft cores, Core and SoC design examples.

MODULE-2

UNIT-1: **[8L+8T+0P=16 Hours]**

DESIGN METHODOLOGY FOR MEMORY AND ANALOG CORES: Embedded memories, Simulation modes specifi cation of analogue circuits, A to D converters, Phase locked loops, High speed I/O.

UNIT-2: **[8L+8T+0P=16 Hours]**

DESIGN VALIDATION: Core level validation - Test benches, SoC design validation, Hardware /software co-simulation and coverifi cation; Case study - Validation and testing of SoC. SoC test issues - Testing of digital logic cores, Built in self-test method.

PRACTICES:

- Implementation of SoC concepts.
- Simulation of hard cores.
- Simulation of soft cores.
- SoC test issues.
- Implementing test benches
- Simulation of digital logic cores
- Implementation of BIST

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Understand and analyse the fundamental concepts, methodologies, design issues of System on-Chip	Analyse	1	1, 2, 4, 5, 9, 10, 12
2	Demonstrate testing issues in digital logic cores.	Apply	1	1, 2, 5, 9, 10

3	Apply the knowledge of methods and design issues in hard-core, soft-core process and analogue circuits.	Apply	2	1, 2, 3, 5, 9, 10
4	Analyse the software and hardware simulation and validate it.	Analyse	2	1, 2, 5, 9, 10, 12

TEXT BOOKS:

1. Rochit Rajsuman, "System-on-a-chip: Design and Test", 2nd edition, Santa Clara, CA: Artech House, 2000.
2. Prakash Rashinkar, Peter Paterson and Leena Singh, "System-on-a-chip verification: Methodology and Techniques", 3rd edition, Kluwer Academic Publishers, 2011.

REFERENCE BOOKS:

1. M. Keating, D.Flynn, R.Aitken, A. Gibbons and K. Shi, "Low Power Methodology Manual for System-On-Chip Design Series (Integrated Circuits and Systems)", 2nd edition, Springer, 2007.
2. L.Balado and E. Lupon, "Validation and test of systems on chip", Twelth Annual IEEE conference on ASIC/SOC, 1999.
3. A.Manzone, P.Bernardi, M.Grosso, M.Rebaudengo, E.Sanchez and M.S.Reorda "Integrating BIST techniques for on-line SoC testing", Eleventh IEEE International on line testing symposium, 2005.

22VLXXX – Mixed Signal Design

Hours per Week:

L	T	P	C
3	0	2	**4**

PREREQUISITE COURSE: CMOS Analog IC design.

COURSE DESCRIPTION AND OBJECTIVES:

This course focuses on advanced design approaches for bandgap references, comparators, ADC/DAC, oscillators, and PLL. The objective of the course is to build and implement the product level design blocks for VLSI applications.

MODULE-1

UNIT-1 **[12L+8T+0P=20 Hours]**

Comparator & Multiplier: Characterization of a comparator, Basic CMOS comparator design, analog multiplier

PLL: Simple PLL, charge-pump PLL, applications of PLL

UNIT-2 **[12L+8T+0P=20 Hours]**

Switched Capacitor circuits: Basic principles, switched capacitor sensitive integrator and insensitive integrator, switched capacitor filter, switched capacitor amplifier.

Sample & hold and trans-linear circuits: Performance of sample-and-hold circuits, MOS sample-and-hold basics, examples of CMOS S/H Circuits, trans-linear gain Cell, trans-linear multiplier.

PRACTICES:

- Design and simulate the following mixed signal circuits.
- High speed and high gain comparators.
- PLL
- Switched Capacitor circuits.
- Sample and Hold circuit.

MODULE-2

UNIT-1 **[12L+8T+0P=20 Hours]**

Analog CMOS Filters: Low Pass filters, active–RC fully differential integrator, Two transistor MOSFET– C integrator, gm-C Integrator, Active RC integrators.

Data converters specifications: Ideal D/A converter, ideal A/D converter, quantization noise, performance metrics, resolution, offset and gain error, accuracy, and linearity.

UNIT-2 **[12L+8T+0P=20 Hours]**

D/A Converter architectures: Resistor-Ladder architectures, Capacitive DAC, Cyclic DAC, current-steering, Pipeline DAC.

A/D converter architectures: Flash architectures, interpolate and folding architectures, pipelined architectures, Ramp type ADC, Integrating (Dual slope) ADC, Successive approximation architectures, Sigma Delta ADC, Design of Decimation filter.

PRACTICES:

- Design and simulate the following mixed signal circuits.
- First order filter
- gm-C Integrator
- Capacitive DAC
- Flash ADC

SKILLS:

- Identify and analyze various switched capacitor circuits.
- Design of phase locked loops.
- Analyze the performance of ADC's & DAC's.

ACTIVITIES:

- Advanced CMOS analog IC design.
- Design of oscillators and phase lock loop circuit.
- Analyze the signal to noise ratio and modeling of mixed signals.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Analyze CMOS based comparator and PLL.	Analyze	1	1, 2, 4, 5, 9, 10, 12
2	Use the techniques and skills for designing CMOS based switched capacitor circuits	Apply	1	1, 2, 3, 5, 9, 10
3	Able to enhance the performance of sampling circuits.	Apply	1	1, 2, 5, 9, 10
4	Design the frequency and Q tunable time domain filters	Apply	2	1, 2, 3, 5, 9, 10
5	Identify, formulates, and solves engineering problems in data converters of mixed-signal design	Analyze	2	1, 2, 5, 9, 10, 12

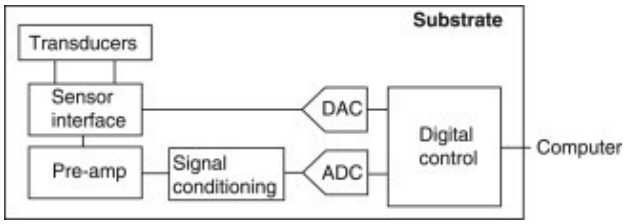
TEXTBOOKS:

1. B.Razavi, *"*Design of analog CMOS integrated circuits*"*, McGraw Hill, 2001.
2. B.Razavi, *"*Principles of data conversion system design*"*, S.Chand and company ltd, 2000.
3. Jacob Baker et. all, "
4. Mixed-Signal circuit design", IEEE Press, 2002

REFERENCE BOOKS:

1. Gregorian, Temes, "Analog MOS Integrated Circuit for signal processing", John Wiley & Sons.
2. Schreier & Themes, Understanding Delta-Sigma Data Converters, Wiley –IEEE Press, 2004.

Image source: https://www.sciencedirect.com/topics/computer-science/data-converter


Substrate
Transducers
Sensor interface
Pre-amp
Signal conditioning
DAC
ADC
Digital control
Computer

22VLB809 – CMOS RF INTEGRATED CIRCUITS

Hours per Week:

L	T	P	C
2	2	0	**3**

PREREQUISITE KNOWLEDGE: Knowledge on Analog IC Design, Communication Theory.

COURSE DESCRIPTION AND OBJECTIVES:

This course introduce the principles, analysis, and design of CMOS Radio frequency (RF) integrated circuits for wireless communication systems. This course also present rule-of-thumbs in designing RF main blocks such as Low-Noise-Amplifier (LNA), mixer, Voltage-controlled-oscillator (VCO), and Power amplifier.

MODULE-1

UNIT-1: BASIC CONCEPTS IN RF DESIGN [8L+4T=16 Hours]

Basic concepts in RF design- Nonlinearity, Noise, Sensitivity, Dynamic range, Impedance transformation, S-parameters. Transmitter architectures and Receiver architectures

UNIT-2: LOW NOISE AMPLIFIERS AND MIXERS [8L+4T=16 Hours]

LNA topologies, Active and passive Mixers

PRACTICES:

- LNA Design
- Mixer Design

MODULE-2

UNIT-1: OSCILLATORS & PHASE-LOCKED LOOPS [8L+4T=16 Hours]

Feedback Oscillators, Cross-coupled Oscillators, Voltage controlled Oscillators, LC VCOs, Quadrature Oscillators, Type-I PLLs, Type-II PLLs and phase noise in PLLs

UNIT-2: POWER AMPLIFIERS [8L+4T=16 Hours]

High Efficiency Power amplifiers, Basic Linearization techniques, Doherty power amplifiers

PRACTICES:

- Low-Noise VCOs
- Cascode PA
- Positive-feedback PAs
- PAs with power combining\
- Design of PLLs

SKILLS:

- Receiver Design-LNA, Mixer, AGC
- TX Design-PA, Upconverter
- Synthesizer Design- VCO, Divider, loop Design

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Understand fundamental RF circuit theory and design	Understanding	1	1, 2, 4, 5, 9, 10, 12
2	Able to design and analyze CMOS RF LNAs and Mixers	Analyze	1	1, 2, 3, 5, 9, 10
3	Design and analyze CMOS RF Oscillators	Analyze	2	1, 2, 5, 9, 10
4	Synthesis of PLL for transceiver design	Evaluate	2	1, 2, 3, 5, 9, 10

Text Books: (

1. Thomas H. Lee ,"The Design of CMOS Radio-Frequency Integrated Circuits". 2nd ed, Cambridge University Press, 2012.

2. Behzad Razavi ,"RF Microelectronics". 2nd ed, Prentice Hall, 2011.

Reference Books:

1. A.A. Abidi, P.R. Gray, and R.G. Meyer," Integrated Circuits for Wireless communications", New York: IEEE Press, 1999.

2. Jeremy Everard, "Fundamentals of RF Circuit Design With Low Noise Oscillators",John Wiley & Sons Ltd.2001

22VLB810 – MEMS & NEMS

Hours per Week:

L	T	P	C
2	2	0	**3**

COURSE OBJECTIVE:

- To introduce the concepts of micro and nano electromechanical devices
- To know the fabrication process of Microsystems
- To know the design concepts of micro sensors and micro actuators
- To introduce the concepts of quantum mechanics and nano systems

MODULE-1

UNIT-1 INTRODUCTION TO MEMS AND NEMS

Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Materials for MEMS and NEMS: Silicon, silicon compounds, polymers, metals.

UNIT-2 MEMS FABRICATION TECHNOLOGIES

Photolithography, Ion Implantation, Diffusion, Oxidation, CVD, Sputtering Etching techniques, Micromachining: Bulk Micromachining, Surface Micromachining, LIGA.

MODULE-2

UNIT-I MICRO SENSORS and ACTUATORS

MEMS Sensors: Design of Acoustic wave sensors, Vibratory gyroscope, Capacitive Pressure sensors, Case study: Piezoelectric energy harvester Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces, Case Study:RF Switch.

UNIT-2 NANO DEVICES

Atomic Structures and Quantum Mechanics, Shrodinger Equation, ZnO nanorods based NEMS device: Gas sensor.

COURSE OUTCOMES:

CO1: Interpret the basics of micro/nano electromechanical systems including their applications and advantages
CO2: Recognize the use of materials in micro fabrication and describe the fabrication processes including surface micromachining, bulk micromachining, and LIGA.
CO3: Analyse the key performance aspects of electromechanical transducers including sensors and actuators
CO4: Applied the knowledge of various micro actuators
CO5: Application of various actuators
CO6: Comprehend the theoretical foundations of quantum mechanics and Nano systems

REFERENCES:

1. Marc Madou, ―Fundamentals of Microfabrication‖, CRC press 1997.
2. Stephen D. Senturia,‖ Micro system Design‖, Kluwer Academic Publishers,2001
3. Tai Ran Hsu ,‖MEMS and Microsystems Design and Manufacture‖ ,Tata Mcraw Hill, 2002.
4. Chang Liu, ―Foundations of MEMS‖, Pearson education India limited, 2006,
5. Sergey Edward Lyshevski, ―MEMS and NEMS: Systems, Devices, and Structures‖ CRC Press, 2002

23VLB811 – ASIC DESIGN

Hours per Week:

L	T	P	C
2	2	-	**3**

PREREQUISITE COURSE: VLSI Design.

COURSE DESCRIPTION AND OBJECTIVES:

- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.
- To give the student an understanding of issues and tools related to ASIC/FPGA design and implementation.
- To give the student an understanding of basics of System on Chip and platform-based design.

MODULE-1

UNIT-1: Types of ASICs

[8L+8T+0P=16 Hours]

Types of ASICs, VLSI Design flow, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Latest Version- FPGAs and CPLDs and Soft-core processors.

UNIT-2: Trade off issues at System Level **[8L+8T+0P=16Hours]**

Optimization with regard to speed, area and power, asynchronous and low power system design. ASIC physical design issues, System Partitioning, Power Dissipation, Partitioning Methods. ASIC floor planning, Placement and Routing

MODULE-2

UNIT-1: System-On-Chip Design **[8L+8T+0P=16Hours]**

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, On-Chip Communication Architecture Standards, Low-Power SoC Design.

UNIT-2: High performance algorithms for ASICS/ SoCs **[8L+8T+0P=16 Hours]**

High performance algorithms for ASICS/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC, USB controllers, OMAP

SKILLS:

- Techniques for designing and verifying digital ASICs.
- Detailed understanding of the entire ASIC design flow.

ACTIVITIES:

- Construct an SRAM memory cell.
- Implement ASIC floor planning, routing, and placement for an adder design.
- Design of an ADC's digital filter

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Demonstrate VLSI tool-flow and appreciate FPGAarchitecture.	Understanding	1	1, 2, 3,4, 5, 9, 10, 12
2	:Understand the issues involved in ASIC design, including technology choice, design management, tool-flow, verification, debugand test, as well as the impact of technology scaling on ASIC design	Apply	1	1, 2, 3,4, 5, 9, 10, 12
3	Understanding and the algorithms used for ASIC construction	Apply	1,2	1, 2, 3,4, 5, 9, 10, 12
4	Understanding and the basics of System on Chip, on chip communication architectures like AMBA, AXI and utilizing Platform based design	Apply	2	1, 2, 3,4, 5, 9, 10, 12
5	Appreciate high performance algorithms available for ASICs IC	Apply	2	1, 2, 3,4, 5, 9, 10, 12

TEXT BOOKS:

1. M.J.S. Smith,"ApplicationSpecific Integrated Circuits", Pearson, 2003 2.
2. H.Gerez, "Algorithms for VLSI Design Automation", John Wiley,1999..

REFERENCE BOOKS:

1. J..M.Rabaey, A. Chandrakasan, and B.Nikolic, "Digital Integrated Circuit Design Perspective (2/e)", PHI 2003.
2. D.A.Hodges,"AnalysisandDesignofDigitalIntegratedCircuits(3/e)", MGH 2004.
3. 3. Hoi-Jun Yoo, KangminLeeandJun Kyong Kim, "Low-Power NoC for High-Performance SoC Design", CRC Press, 2008.
4. S. Pasricha and N. Dutt," OnChipCommunication Architectures System on Chip Interconnect Elsveir", 2008.

22VLB812 – SENSORS AND SENSOR CIRCUIT DESIGN

Hours per Week:

L	T	P	C
2	2	-	**3**

PREREQUISITE COURSE: VLSI Design.

COURSE DESCRIPTION AND OBJECTIVES:

- Introduce the sensor used in the industries and their characteristics, properties, interfaces connection
- Students learn how to analyze, design, build and troubleshoot a variety of sensor circuit

MODULE-1

UNIT-1: REVIEW OF MEASUREMENTS AND INSTRUMENTATION

[8L+8T+0P=16 Hours]

Review of Static characteristics of Instrument systems, dynamic characteristics of Instrument systems, Review of Op-Amp Circuit, passive-, and active-filters.

UNIT-2: ANALOG SIGNAL CONDITIONING [8L+8T+0P=16Hours]

Principles of analog signal conditioning, Signal-Level and Bias Changes, Linearization, Conversions, Filtering and Impedance Matching, Concept of Loading, PASSIVE CIRCUITS: Voltage Divider, Bridge Circuits, Bridge Resolution , Bridge Applications

MODULE-2

UNIT-1: DIGITAL SIGNAL CONDITIONING [8L+8T+0P=16Hours]

Review of Digital Electronics: Digital Information, Fractional Binary Numbers, Boolean Algebra, Digital Electronics Circuits: comparator, converter, Digital-to-Analog Converters (DACs), Analog-to-Digital Converters (ADCs) : Flash-, SAR, Dual Slope, Sensor-to-Frequency Conversion, Data-Acquisition Systems: Hardware and Software of Data Aquisition System (DAS), Characteristics of digital data: Digitized Value, Sampled Data Systems, Linearization,

UNIT-2: THERMAL SENSORS [8L+8T+0P=16 Hours]

Definition of Temperature: Thermal Energy, absolute and relative Temperature, Metal resistance versus temperature devices: Resistance versus Temperature Approximations, Resistance-Temperature Detectors (RTD), Other thermal sensor: Bimetal Strips, Gas Thermometers, Vapor-Pressure Thermometers, Liquid-Expansion Thermometers, Solid-State Temperature Sensors, Design considerations

SKILLS:

- Knowledge on basic building blocks of electronics for designing sensors.
- Able to integrate sensors to the application.

ACTIVITIES:

Design sensors for a variety of purposes and connect them to the appropriate circuits.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Understand the basic concepts of op-amp and filters for sensor circuits	Understanding	1	1, 2, 3,4, 5, 9, 10, 12
2	Analysing various sensor circuit performances along with application	Apply	1	1, 2, 3,4, 5, 9, 10, 12
3	Integrate the various circuits for sensors for analysing the performance	Apply	1,2	1, 2, 3,4, 5, 9, 10, 12
4	Understand the basic concepts of signal conditioning circuits	Apply	2	1, 2, 3,4, 5, 9, 10, 12
5	:Integrated the sensors with corresponding circuits.	Apply	2	1, 2, 3,4, 5, 9, 10, 12

TEXT BOOKS:

1. "Process Control Instrumentation Technology, 6th Edition", Author: Curtis D. Johnson, Publisher: Prentice Hall International Edition.
2. "Measurement, Instrumentation, and Sensors Handbook", Author/Chief Editor: John G. Webster., Publisher: CRC – Press – Taylor and Francis Group.

REFERENCE BOOKS:

4. Introduction to Instrumentation and Measurement, 3rd Edition", Authors: Robert B. Northrop, Publisher: CRC – Press – Taylor and Francis Group.

22VLB813 – VLSI SIGNAL PROCESSING

L	T	P	C
2	2	-	3

COURSE OBJECTIVE:

- Introduce students to the fundamentals of VLSI signal processing and expose them to examples of applications.
- Design and optimize VLSI architectures for basic DSP algorithms.
- Design and optimize VLSI architectures for basic DSP algorithms.

MODULE-I

UNIT-1 **10 hours**

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques.

UNIT-2 **10 hours**

Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems.

MODULE-2

UNIT-1 **10 hours**

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays.

UNIT-2 **10 hours**

Fast Convolution: Introduction, Cook, Toom Algorithm, Winogard Algorithm,Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

TEXT BOOKS:

1. Keshab K. Parhi. VLSI Digital Signal Processing Systems, Wiley-Inter Sciences, 1999
2. Mohammed Ismail, Terri, Fiez, Analog VLSI Signal and Information Processing, McGraw Hill, 1994.
3. Kung. S.Y., H.J. While house T.Kailath, VLSI and Modern singal processing, Prentice Hall, 1985.
4. Jose E. France, YannisTsividls, Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing Prentice Hall, 1994.

COURSE OUTCOMES:

1. Understand VLSI design methodology for signal processing systems.
2. Be familiar with VLSI algorithms and architectures for DSP.
3. Be able to implement basic architectures for DSP using CAD tools.

ADD-ON DEGREE COURSES

22VLB951 – NANO ELECTRONIC DEVICES AND DEVICE MODELLING

Hours per Week:

L	T	P	C
2	2	0	3

PREREQUISITE KNOWLEDGE: Basic knowledge of Solid-State Devices and VLSI

COURSE DESCRIPTION AND OBJECTIVES:

The goal of this course is to provide an insight into the fundamentals of Nanoscience and nanotechnology. The course provides basics of nanomaterials, quantum mechanics and statistical mechanics

MODULE-1

UNIT-1 **[6L+6T+0P=12 Hours]**

Introduction to Nanotechnology: Importance of Nanotechnology, Opportunity at the nano scale, length and time scale in structures, Classification of Nanostructures, Limitations of conventional microelectronics, Low dimensional structures Quantum wells, wires and dots, Density of states and dimensionality, Properties of two dimensional semiconductor nanostructures, square quantum wells of finite depth, parabolic and triangular quantum wells, Quantum wires and quantum dots, Carbon nanotube, Graphene; Trends in microelectronics and optoelectronics.

Basic of Quantum Mechanics: Introduction to Quantum Mechanics - Schrodinger equation – time dependent and time independent equations. Solutions of the Schrodinger equation – free particle - particle in a box – one and three dimensions - particle in a finite well - Penetration through a barrier – Tunnel effect – Single step barrier.

UNIT-2 **[10L+10T+0P=20 Hours]**

Fabrication Methodologies

Introduction to methods of fabrication of nano-layers, different approaches, physical vapour deposition, chemical vapour deposition, Molecular Beam Epitaxy, Ion Implantation, Formation of Silicon Dioxide- dry and wet oxidation methods, Fabrication of nano particle- grinding with iron balls, laser ablation, reduction methods, sol gel, self-assembly, precipitation of quantum dots.

MODULE-2

UNIT-1 **[6L+6T+6P=12 Hours]**

Mathematical Modelling for Electron & Characterization techniques

Modelling: Transport of charge in Nanostructures under Electric field - parallel transport, hot electrons, perpendicular transport, Quantum transport in nanostructures, Coulomb blockade, Transport of charge in magnetic field - Effect of magnetic field on a crystal. Aharonov-Bohm effect, the Shubnikov-de Hass effect, the quantum Hall effect.

Characterization: Introduction to characterization of nanostructures, tools used for of nano materials characterization, microscope-optical, electron, and electron microscope, Principle of operation of Scanning Tunnelling Microscope, Atomic Force Microscope, Scanning Electron microscope, Specimen interaction. Transmission Electron Microscope,X-Ray Diffraction analysis, PL & UV Spectroscopy, Particle size analyser.

UNIT-2: **[10L+10T+0P=20 Hours]**

MODFETS, heterojunction bipolar transistors, Resonant tunnel effect, RTD, RTT, Hot electron transistors, Coulomb blockade effect and single electron transistor, CNT transistors, Heterostructure semiconductor laser, Quantum well laser, quantum dot LED, quantum dot laser, Quantum well optical modulator, quantum well sub band photo detectors, principle of NEMS.

COURSE OUTCOMES:

At the end of the course, the students should be able to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	**The** students will be able to understand basic concepts of nanoelectronics devices and nano technology	Understanding	1,2	1, 2, 3, 4, 9, 10, 11, 12
2	To understand and familiarize the quantum, Mechanics.	Understanding	1,2	1, 2, 3, 4, 9, 10, 11, 12
3	To provide the recent advancement of fabrication technologies	Application	1,2	1, 2, 3, 4, 9, 10, 11, 12
4	To provide basic understanding of nanoelectronics devices.	Analysing	1,2	1, 2, 3, 4, 9, 10, 11, 12

BOOKS AND REFERENCES:

TEXT BOOK:

1. T. Pradeep ―A textbook of Nanoscience and Nanotechnology, Tata McGraw – Hill education private ltd, 2012.
2. David. J, Griffiths, ―Introduction to Quantum Mechanics", Pearson, 2009
3. Richard. L, Liboff, ―Introductory Quantum Mechanics", Pearson, 2003.
4. J.M. Martinez-Duart, R.J. Martin Palma, F. Agulle Rueda Nanotechnology for Microelectronics and optoelectronics, Elsevier, 2006.
5. W.R. Fahrner, Nanotechnology and Nanoelctronics, Springer, 2005.

REFERENCES:

1. Chattopadhyay, Banerjee, Introduction to Nanoscience & Technology, PHI, 2012
2. George W. Hanson, Fundamentals of Nanoelectronics, Pearson Education, 2009.
3. K. Goser, P. Glosekotter, J. Dienstuhl, Nanoelectronics and nanosystems, Springer 2004.
4. Murty, Shankar, Text book of Nanoscience and Nanotechnology, Universities Press, 2012.

5. Poole, Introduction to Nanotechnology, John Wiley, 2006.
6. Supriyo Dutta, Quantum Transport- Atom to transistor, Cambridge, 2013.

22VLB952- HARDWARE SECURITY

Hours per Week:

L	T	P	C
3	2	-	**4**

PREREQUISITE KNOWLEDGE: Programming Language.

COURSE DESCRIPTION AND OBJECTIVES:

This course will focus on the importance of addressing different security threats on modern hardware design, manufacturing, installation, and operating practices. The course would borrow concepts from diverse fields of study such as cryptography, hardware design, circuit testing, algorithms, and machine learning.

MODULE-1

UNIT-1 **[12L+8T+0P=20 Hours]**

DIFFERENT ISSUES OF HARDWARE SECURITY:

Overview of Different Issues of Hardware Security, **Preliminaries:** Algebra of Finite Fields, Basics of the Mathematical Theory of Public Key Cryptography, Basics of Digital Design on Field-programmable Gate Array (FPGA), Classification using Support Vector Machines (SVMs).

UNIT-2 **[12L+8T+0P=20 Hours]**

HARDWARE SECURITY PRIMITIVES:

Cryptographic Hardware and their Implementation, Optimization of Cryptographic Hardware on FPGA, Physically Unclonable Functions (PUFs), PUF Implementations, PUF Quality Evaluation, Design Techniques to Increase PUF Response Quality.

PRACTICES:

- Get started quickly with Hardware Security Issues
- Set up a development environment for Digital design on FPGA
- Understanding of Cryptographic Hardware Implementation
- Implement Physically Unclonable Functions (PUFs).

MODULE-2

UNIT-1 **[12L+8T+0P=20 Hours]**

SIDE-CHANNEL ATTACKS ON CRYPTOGRAPHIC HARDWARE: Basic Idea, Current-measurement based Side-channel Attacks (Case Study: Kocher's Attack on DES), Design Techniques to Prevent Side-channel Attacks.

TESTABILITY AND VERIFICATION OF CRYPTOGRAPHIC HARDWARE: Fault-tolerance of Cryptographic Hardware, Fault Attacks, Verification of Finite-field Arithmetic Circuits.

UNIT-2 **[12L+8T+0P=20 Hours]**

MODERN IC DESIGN, MANUFACTURING PRACTICES AND THEIR IMPLICATIONS: Hardware Intellectual Property (IP) Piracy and IC Piracy, Design Techniques to Prevent IP and IC Piracy, Using PUFs to prevent Hardware Piracy, Model Building Attacks on PUFs (Case Study: SVM Modeling of Arbiter PUFs, Genetic Programming based Modeling of Ring Oscillator PUF).

PRACTICES:

- Running Testcases for Verification of Cryptographic Hardware.
- Analyzing simple Fault attacks.
- Understanding Hardware IP Piracy and IC Piracy
- Solving different Case studies

SKILLS:

- Apply the knowledge of Hardware securities and primitives.
- Analyze the different attacks on Cryptographic Hardware.
- Resolve security issues in a Hardware.

ACTIVITIES:

- Creating new case studies for Hardware Security.
- Study IC design for Verification of Hardware Security.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	Interpret different hardware security problems.	Apply	1	1, 2, 12
2	Implement various Cryptographic Hardware.	Apply	1	1, 2, 5, 12
3	Analyze Testability and Verification of Cryptographic Hardware	Analyze	2	1, 2, 3, 5, 12
4	Analyze Modern IC Design and Manufacturing process.	Analyze	2	1, 2, 12

TEXT BOOKS:

1. Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security: Design, Threats, and Safeguards", CRC Press, 2014.

REFERENCE BOOKS:

1. Ahmad-Reza Sadeghi and David Naccache, "Towards Hardware-intrinsic Security: Theory and Practice", Springer, 2010.
2. Ted Huffmire, "Handbook of FPGA Design Security", Springer, 2014.
3. Stefan Mangard, Elisabeth Oswald, Thomas Popp, "Power analysis attacks - revealing the secrets of smart cards",Springer 2007.
4. Doug Stinson, "Cryptography Theory and Practice", CRC Press, 2006.

22VLB953 – LOW POWER VLSI DESIGN

Hours per Week:

L	T	P	C
3	0	2	**4**

PREREQUISITE COURSE: AICD & DICD.

COURSE DESCRIPTION AND OBJECTIVES:

To understand the critical requirements and implementation of Low-power VLSI circuits. The course also covers critical issue related to continuous scaling of microelectronic circuits.

MODULE-1

UNIT-1 **[12L+8T+0P=20 Hours]**

Fundamentals of Low Power VLSI Design: Need for Low Power Circuit Design

Sources of Power Dissipation: Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation

Short Channel Effects: Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT-2 **[12L+8T+0P=20 Hours]**

For achieving low power: Switching activity reduction, algorithmic optimization, architecture optimization, logic optimization, circuit optimization.

Architectural Level Approach: Pipelining and Parallel Processing Approaches.

Different logic styles: Static and dynamic logic, Clock gating, reducing glitching through path balancing, input reordering.

Low-Power Design Approaches: VTCMOS circuits, MTCMOS circuits, Transistor stacking, power gating, Dynamic threshold CMOS.

PRACTICES:

Design and simulate the logic circuits implementing the following low power techniques.

- VTCMOS.
- MTCMOS
- Transistor stacking.
- Power gating.

MODULE-2

UNIT-1 **[12L+8T+0P=20 Hours]**

Low-Voltage Low-Power Design Techniques: Trends of Technology and Power Supply Voltage, Low- Voltage Low-Power Logic Styles, Low-Voltage Low-Power Adders, Low-Voltage Low-Power Multipliers.

UNIT-2 **[12L+8T+0P=20 Hours]**

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre-charge and Equalization Circuit, Low Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

PRACTICES:

- Design and simulate the following circuits.
- Low-Voltage Low-Power Adders
- Low-Voltage Low-Power Multipliers
- Low power SRAM
- Self-refresh circuit of DRAM

SKILLS:

- To design and analyze low power and low voltage circuits.
- To implement existing low power techniques to various designs.
- Able to develop new techniques to reduce power.

ACTIVITIES:

- Implement advanced low power techniques.
- Design of advanced adders and multipliers.
- Improve efficiency of memories in terms of power.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mappingwith POs
1	Acquires knowledge about the second order effects of MOS transistor characteristics.	Underst and	1	1, 2, 4, 5, 9, 10, 12
2	Analyze various CMOS low power design techniques and apply these approaches to various logic circuits.	Analyze	1	1, 2, 3, 4, 5, 9, 10
3	Design and implementation of computational structures for low power applications	Apply	1	1, 2, 3, 5, 9, 10
4	Analyze memories with efficient architectures to improve power.	Analyze	2	1, 2, 4, 5, 9, 10

TEXT BOOKS:

1. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.
2. Anantha P. Chandrakasan, and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publications, 1995.

REFERENCE BOOKS:

1. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley & Sons, 2000.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.
3. Rabaey, and Pedram, Low Power Design Methodologies, Kluwer Academic,1997
4. Philip Allen, and Douglas Holberg, CMOS Analog Circuit Design, Oxford University Press, 2002.

Image source: https://www.indiamart.com/proddetail/low-power-clock-distribution-using-a-current-pulsed-clocked-2933425930.html

Image file name: LPVLSI

1. Implement the VHDL portion of coding for synthesis.
2. Identify the differences between behavioral and structural coding styles.
3. Understand the basic principle of circuit design and analysis.
4. K Jha and S.G Gupta ," Cambridge University Press, 2003

22VLB954- HARDWARE / SOFTWARE CO-DESIGN

Hours per Week:

L	T	P	C
3	2	-	**4**

PREREQUISITE KNOWLEDGE: Computer Architecture.

COURSE DESCRIPTION AND OBJECTIVES:

To analyze and explain the control-flow and data-flow of a software program and a cycle based hardware description. To transform simple software programs into cycle-based hardware descriptions with equivalent behavior and vice versa. To identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components.

MODULE-1

UNIT-1: ISSUES IN CO-DESIGN AND SYNTHESIS [12L+8T+0P=20 Hours]

Co- Design Models, Architectures, Languages, A Generic Codesign Methodology. Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-2: PROTOTYPING & EMULATION [12L+8T+0P=20 Hours]

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure, Architecture Specialization techniques, System Communication infrastructure.

PRACTICES:

- Interfacing Memory to the Processor.
- Interfacing Processor with Peripherals.
- Interfacing a Robot Axis position Control to Processor.

MODULE-2

UNIT-1: COMPILATION TECHNIQUES ANS TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES [12L+8T+0P=20 Hours]

Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT-2: LANGUAGES FOR SYSTEM –LEVEL SPECIFICATION AND DESIGN [12L+8T+0P=20 Hours]

System – level specification, design representation for system level synthesis, system level specification languages. Heterogeneous specifications and multi language co-simulation. Introduction to Cosyma system and LYCOS system.

PRACTICES:

- Study of FPGA Design Test Methodology.
- UART for Software Testing.
- Study of FPGA Hardware Testing Methodology.

SKILLS:

- Use Simulation software to co-simulate software programs with cycle-based hardware description.

ACTIVITIES:

- Design Cosyma & Lycos.
- Simulate cycle based hardware.

COURSE OUTCOMES:

Upon successful completion of this course, students will have the ability to:

CO No.	Course Outcomes	Blooms Level	Module No.	Mapping with POs
1	**Identify** CO Design models.	Apply	1	1, 2, 12
2	**Compare** architecture of control & Data dominated system.	Apply	1	1, 2, 4, 5, 12
3	**Analyze** tools for processor architecture.	Apply	2	1, 2, 3, 5, 12
4	**Design** Cosyma & Lycos system	Create	2	1, 2, 3, 12

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / software co- design Principles and Practice", Springer, 2009.
2. Kluwer, "Hardware / software co- design Principles and Practice", academic publishers,2002.

REFERENCE BOOKS:

1. Rahul Dubay Introduction to Embedded System Design Using Field Programmable Gate Arrays, 2009 Springer-Verlag London Limited.
2. Frank Vahid & Tony Givargis, Embedded System Design, A Unified Hardware/Software Introduction, ISBN 978-0-471-38678-0 2014.